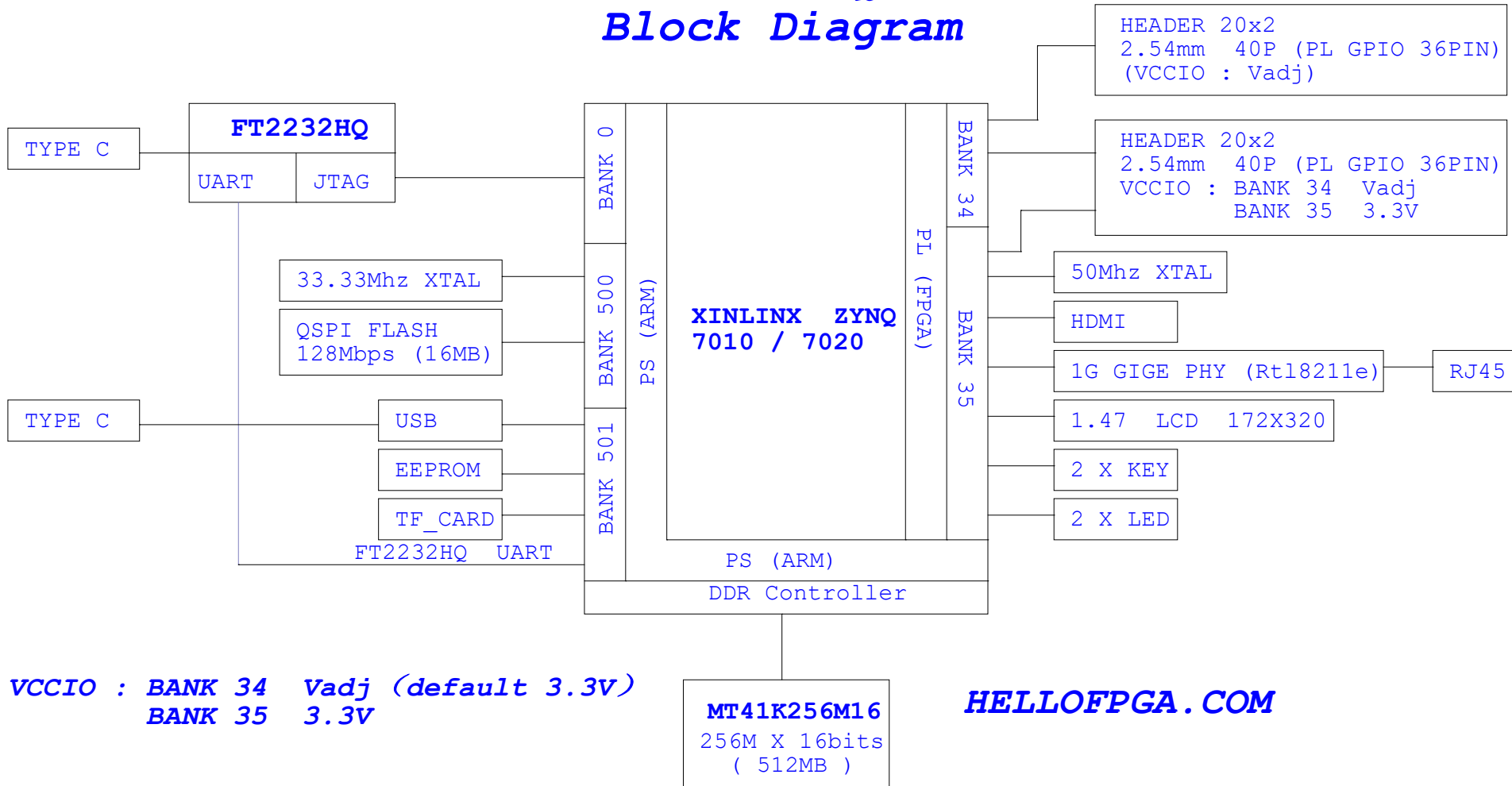
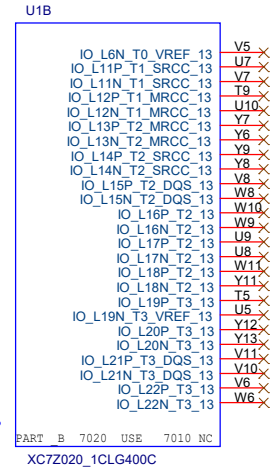
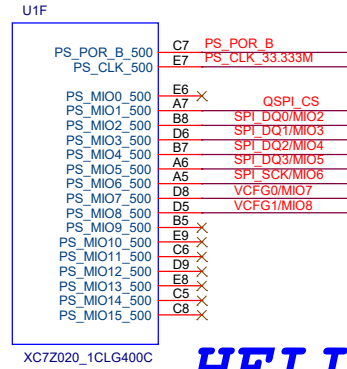
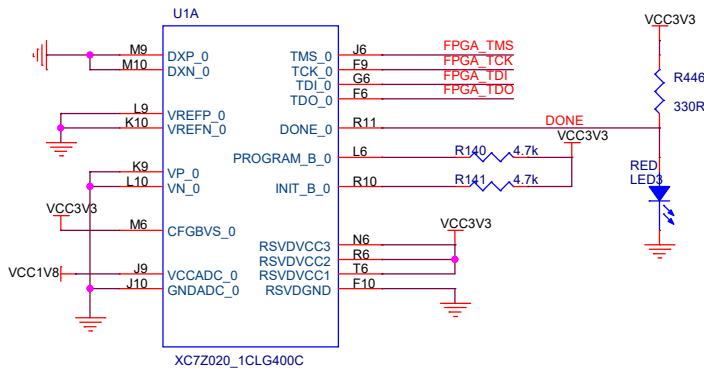
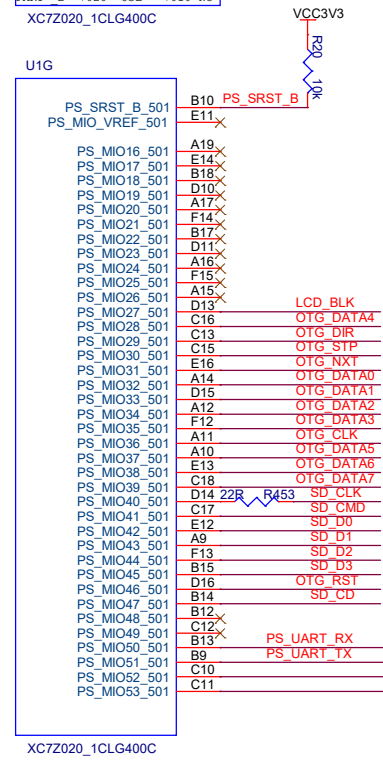
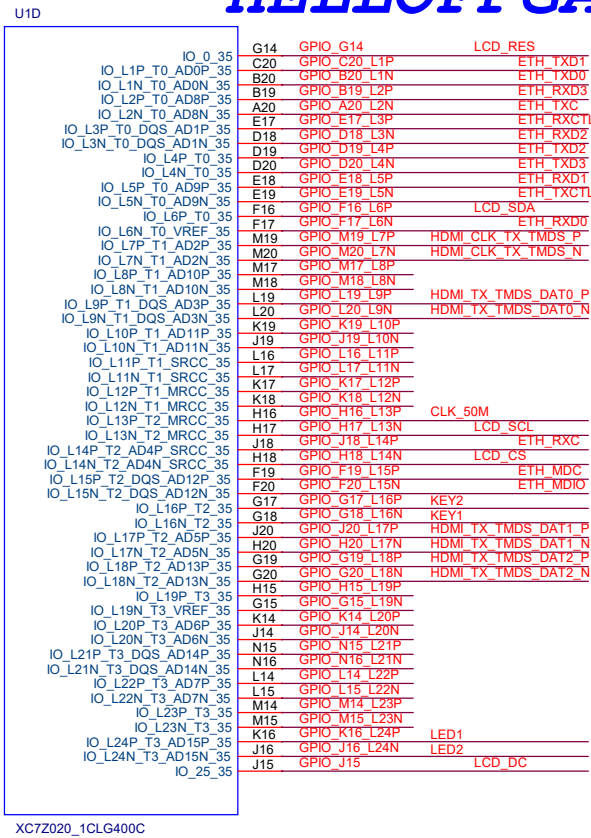
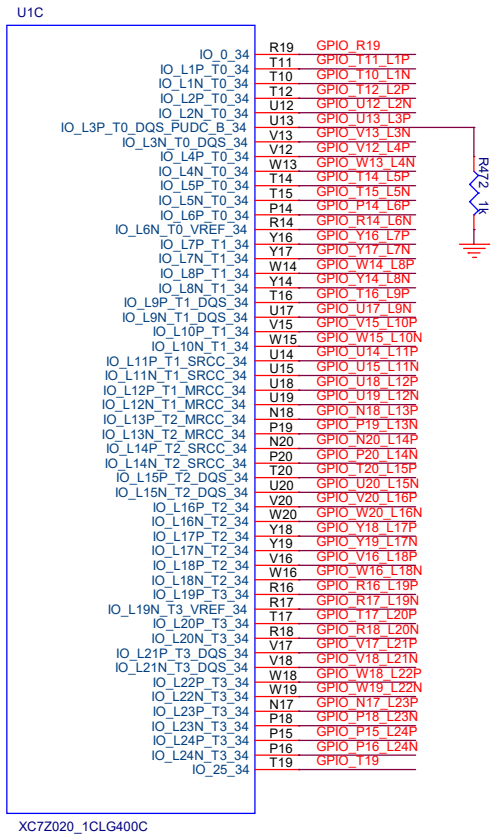


# Smart ZYNQ Block Diagram



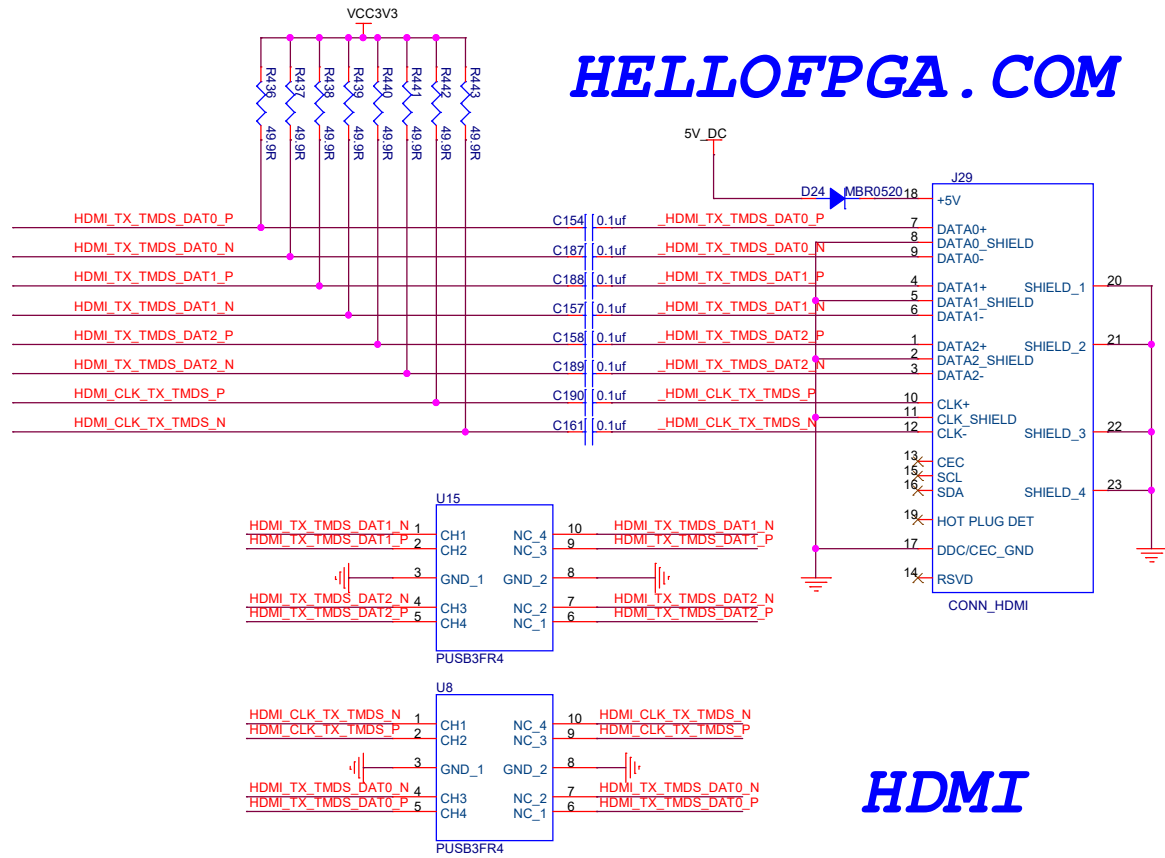


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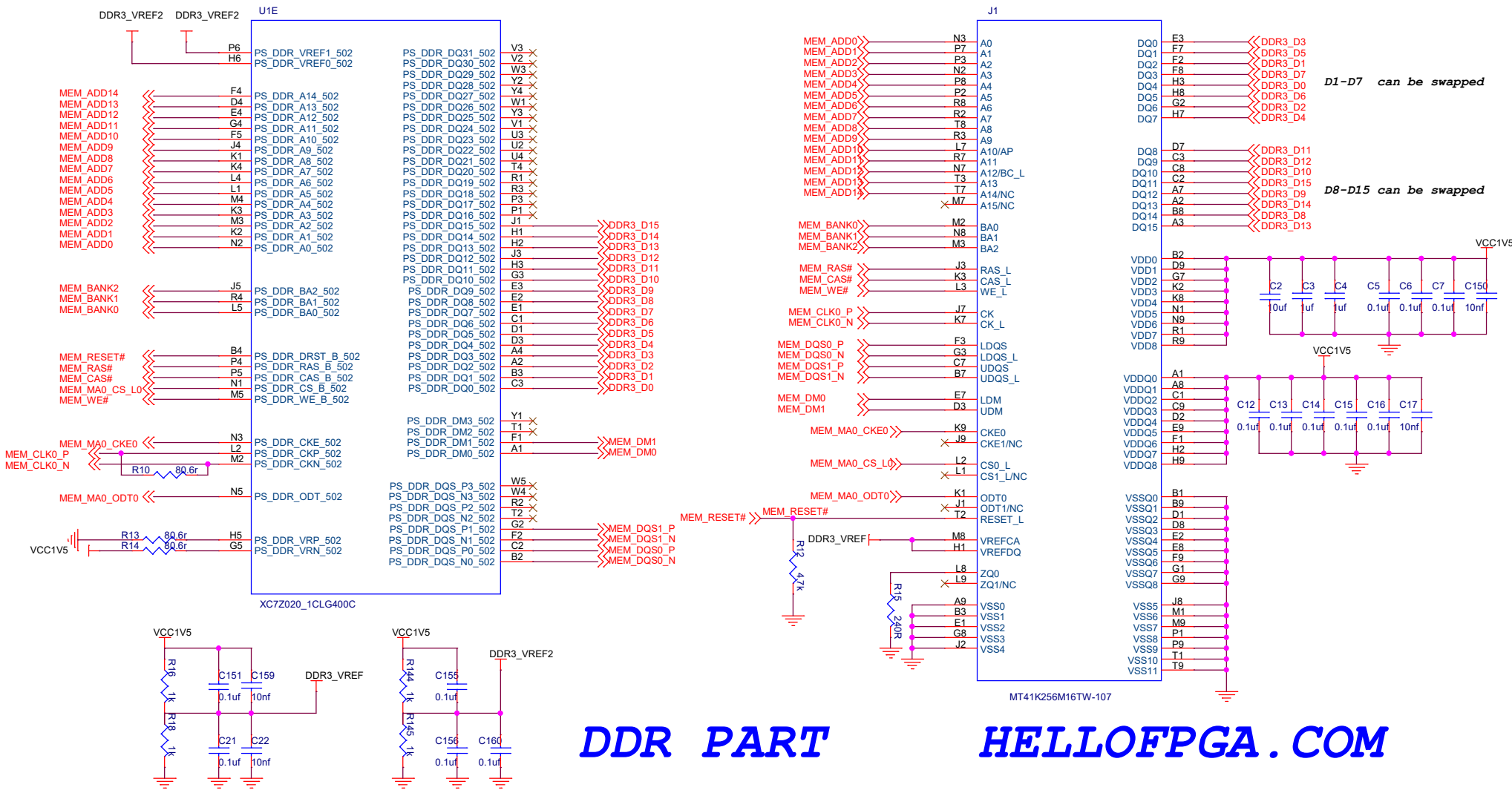
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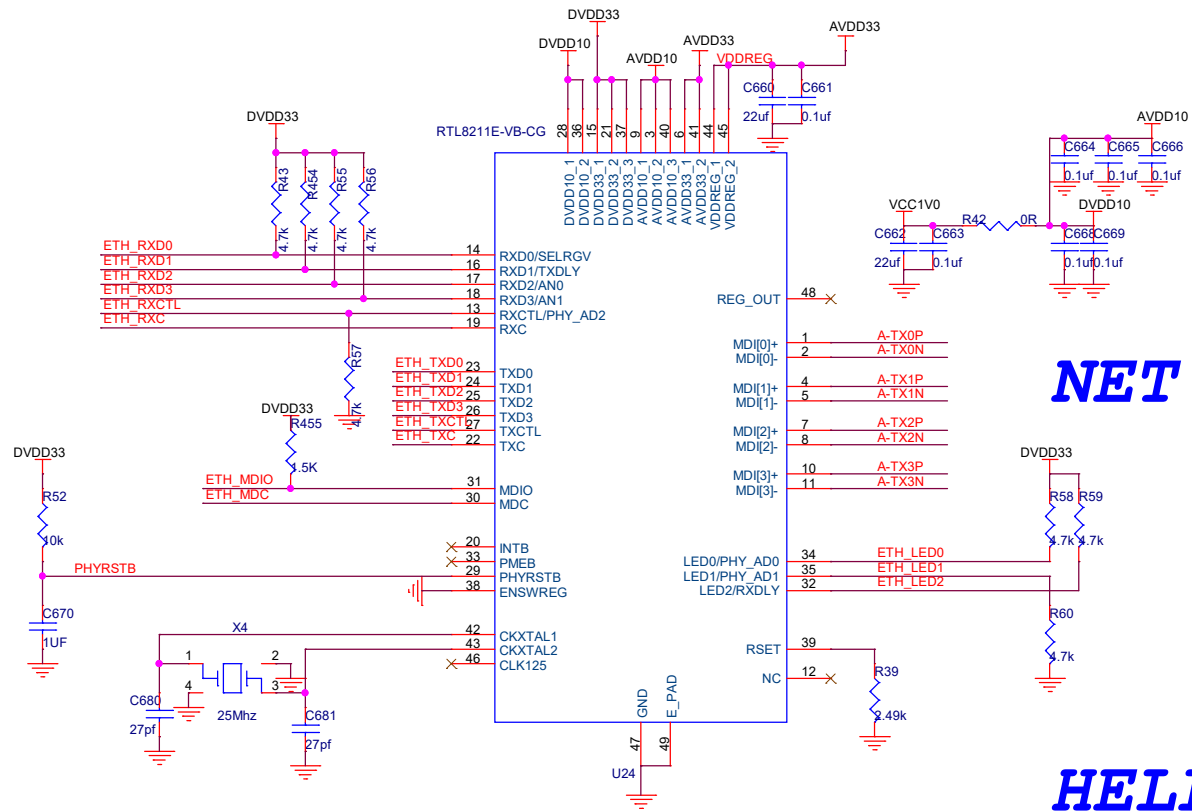


# HDMI

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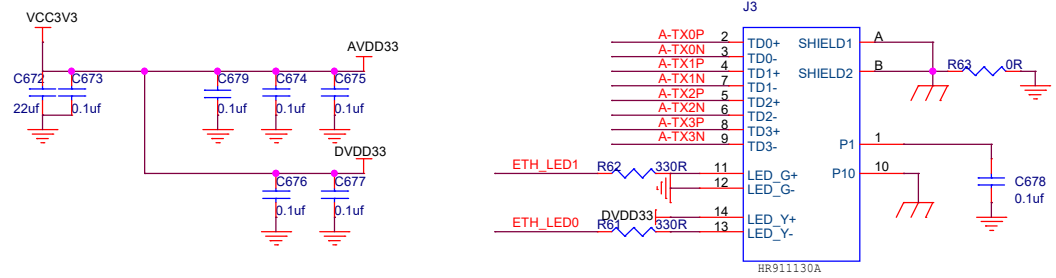


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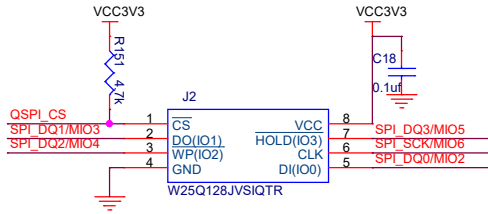
**NET PART**

**HELLOFPGA.COM**

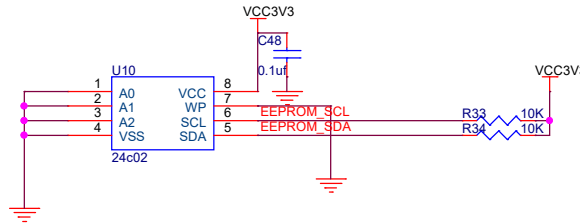


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Date:	Wednesday, January 25, 2023	Sheet 1 of 1

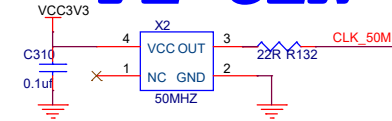
# QSPI FLASH



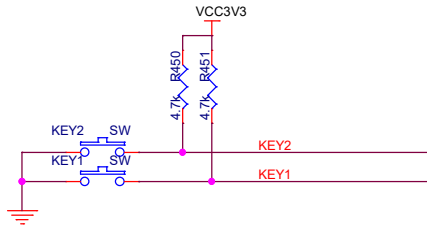
# EEPROM



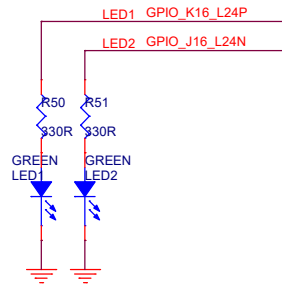
# PL CLK



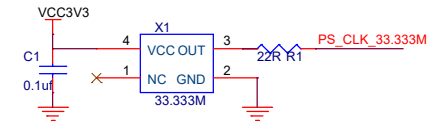
# KEY



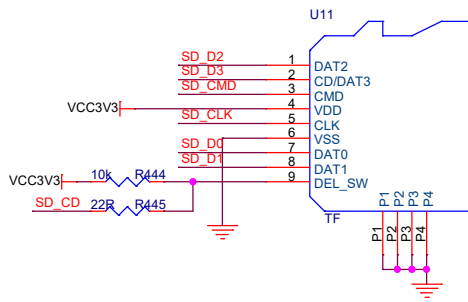
# LED



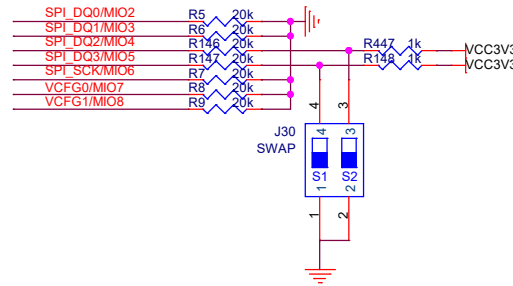
# PS CLK



# TF CARD



# BOOT

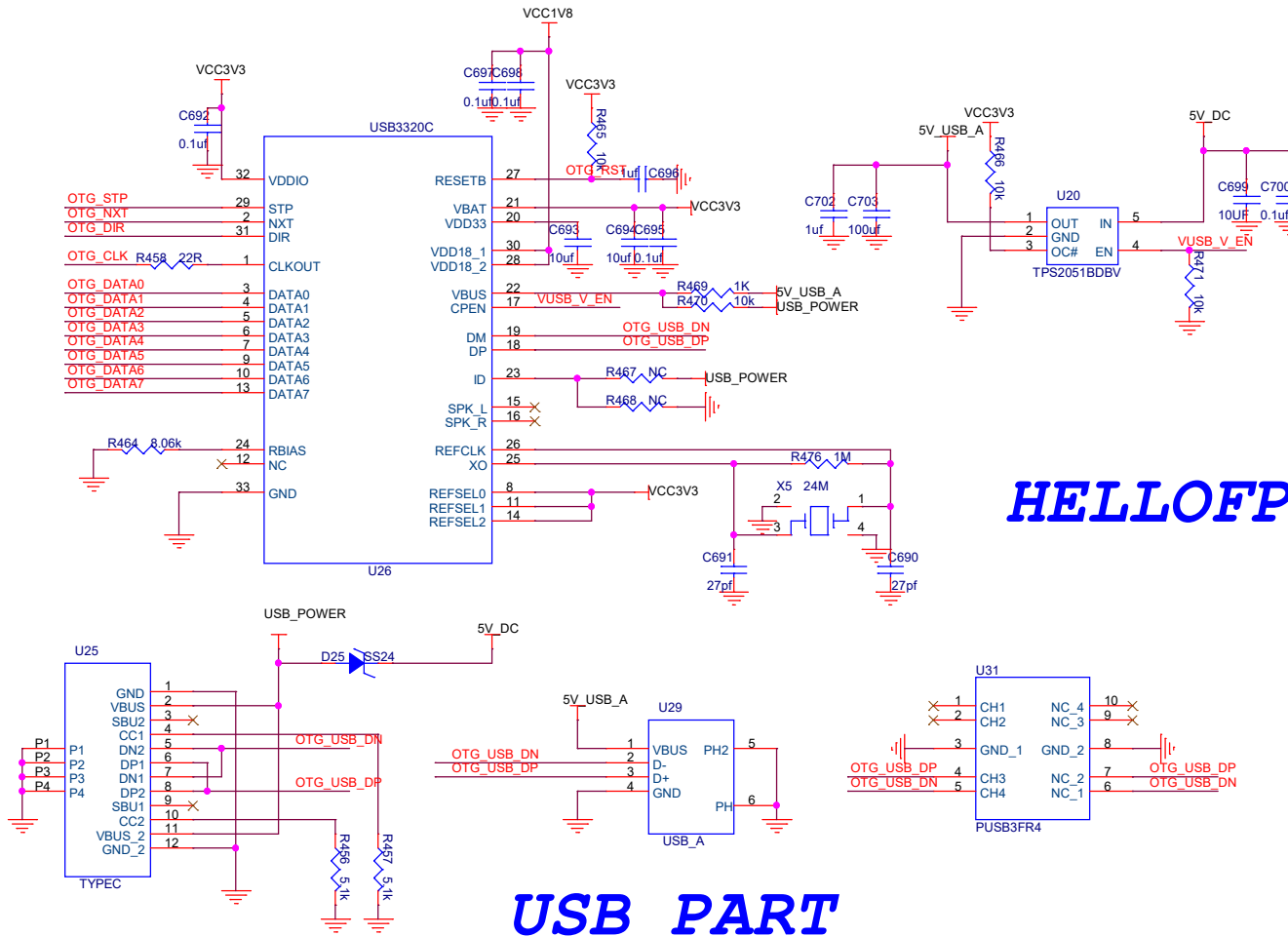


# BOOT

BOOT	S1	S2
JTAG	●	●
QSPI	○	●
SD	○	○

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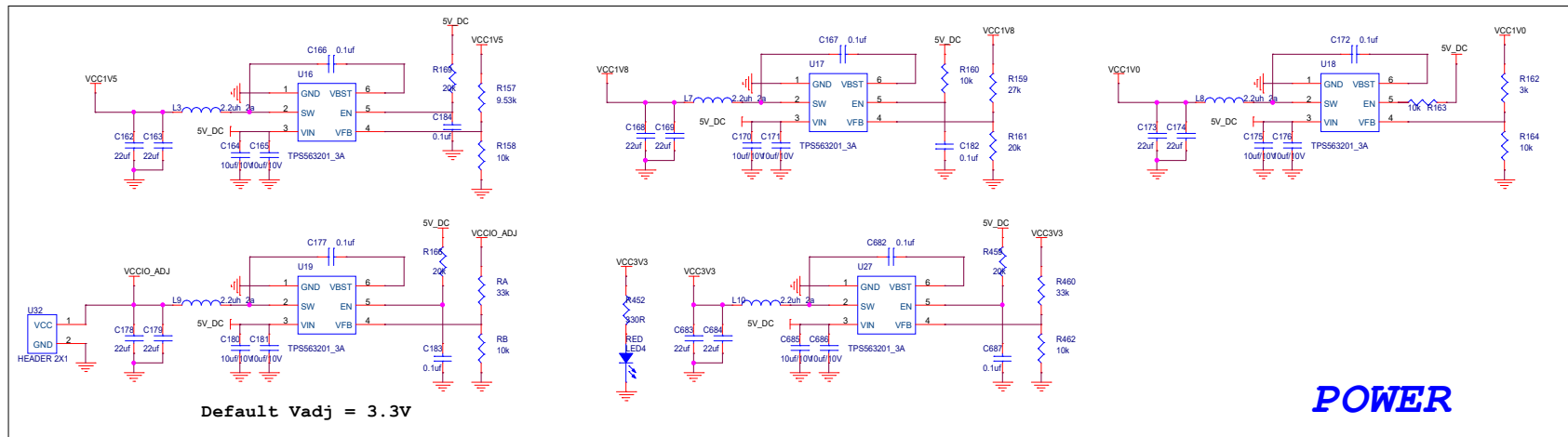
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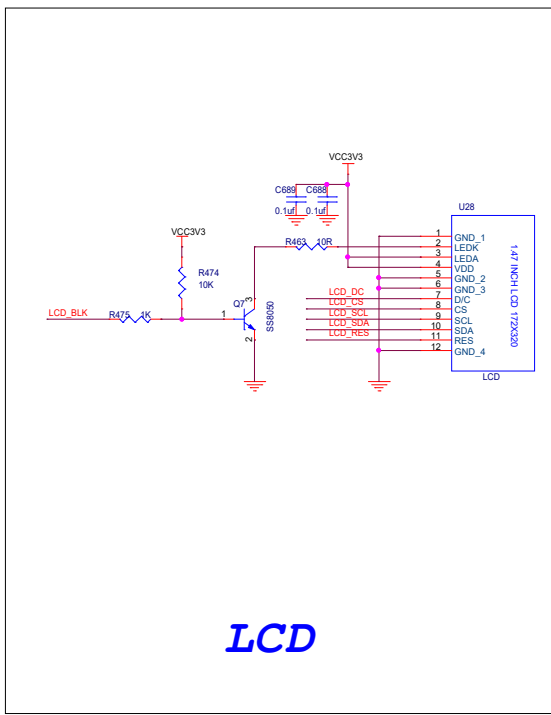
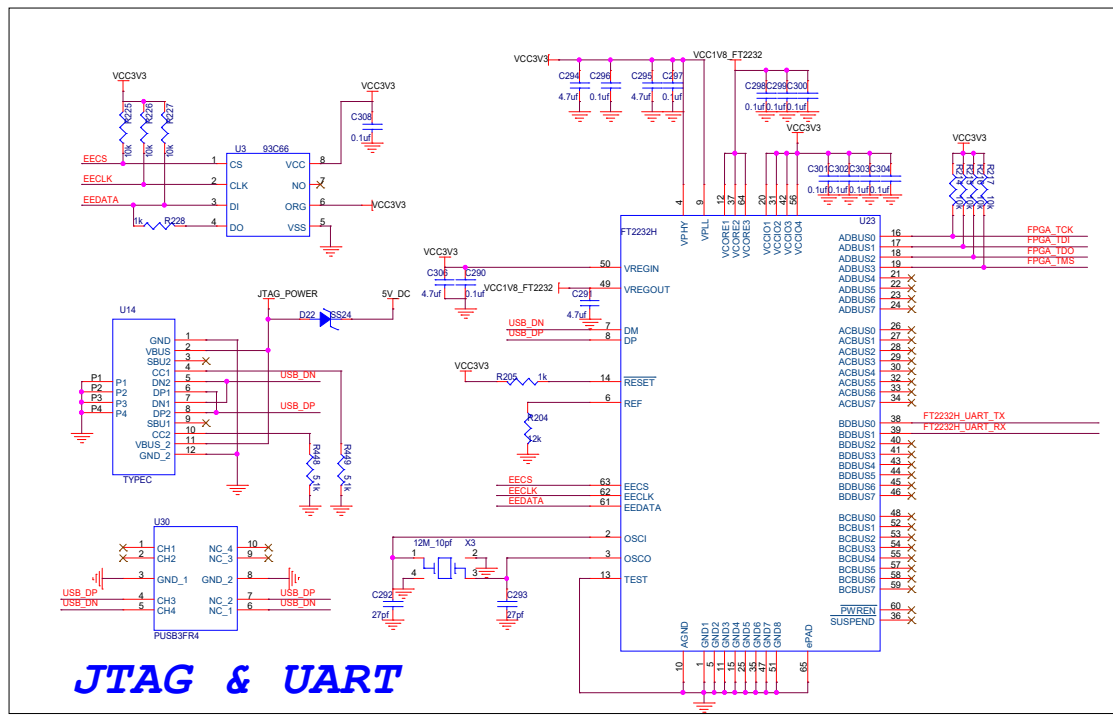
**USB PART**

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Date:	Sunday, February 05, 2023	Sheet 1 of 1

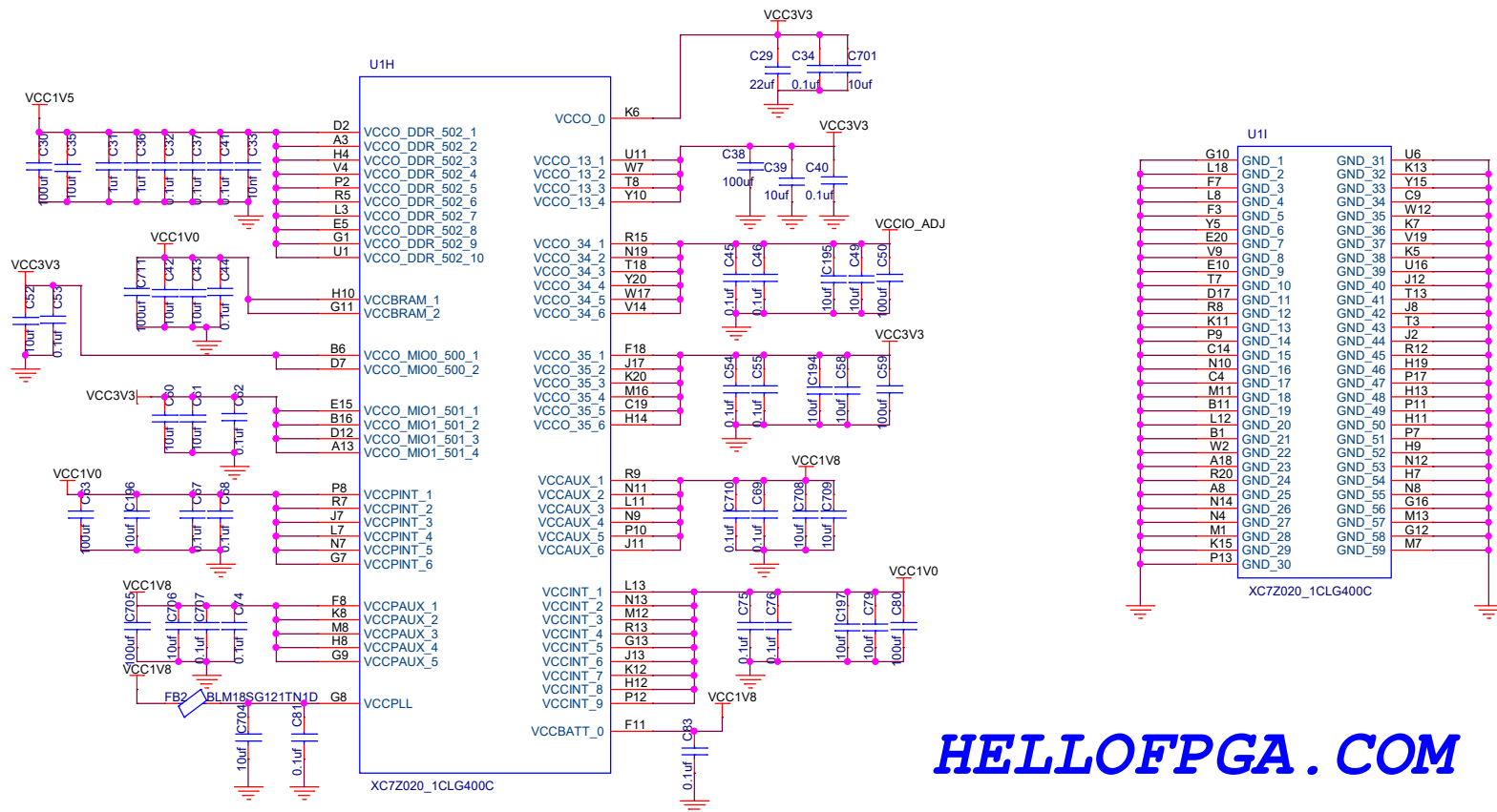


# POWER

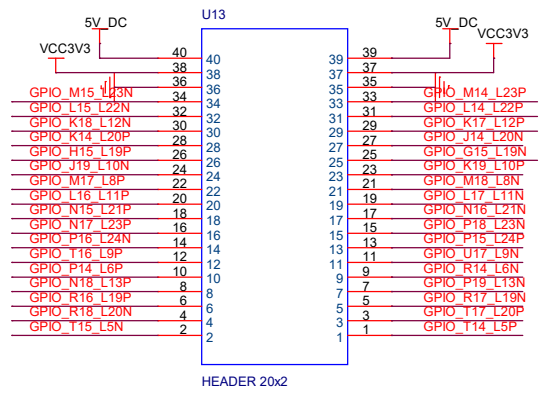
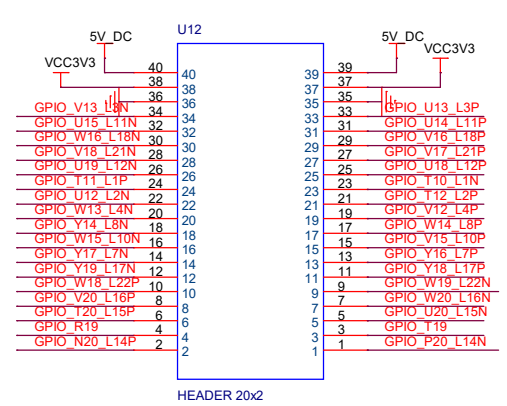
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## HDMI

CLK	M19
D0	L19
D1	J20
D2	G19

## UART

ZYNQ_TX	MIO51
ZYNQ_RX	MIO50

## EEPROM

SCL	MIO52
SDA	MIO53

## 50M CLOCK

CLK	H16
-----	-----

## KEY & LED

KEY1	G18
KEY2	G17
LED1	K16
LED2	J16

## LCD 320X172

LCD_DC	J15
LCD_CS	H18
LCD_SCL	H17
LCD_SDA	F16
LCD_RES	G14
LCD_BLK	MIO27 (PS)

(LCD BLK : default high level by  
External pull-up resistance )

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## GigE phy

ETH TD0	B20
ETH TD1	C20
ETH TD2	D19
ETH TD3	D20
ETH TX_CTL	E19
ETH TXC	A20
ETH RD0	F17
ETH RD1	E18
ETH RD2	D18
ETH RD3	B19
ETH RX_CTL	E17
ETH RXC	J18
ETH MDIO	F20
ETH MDC	F19