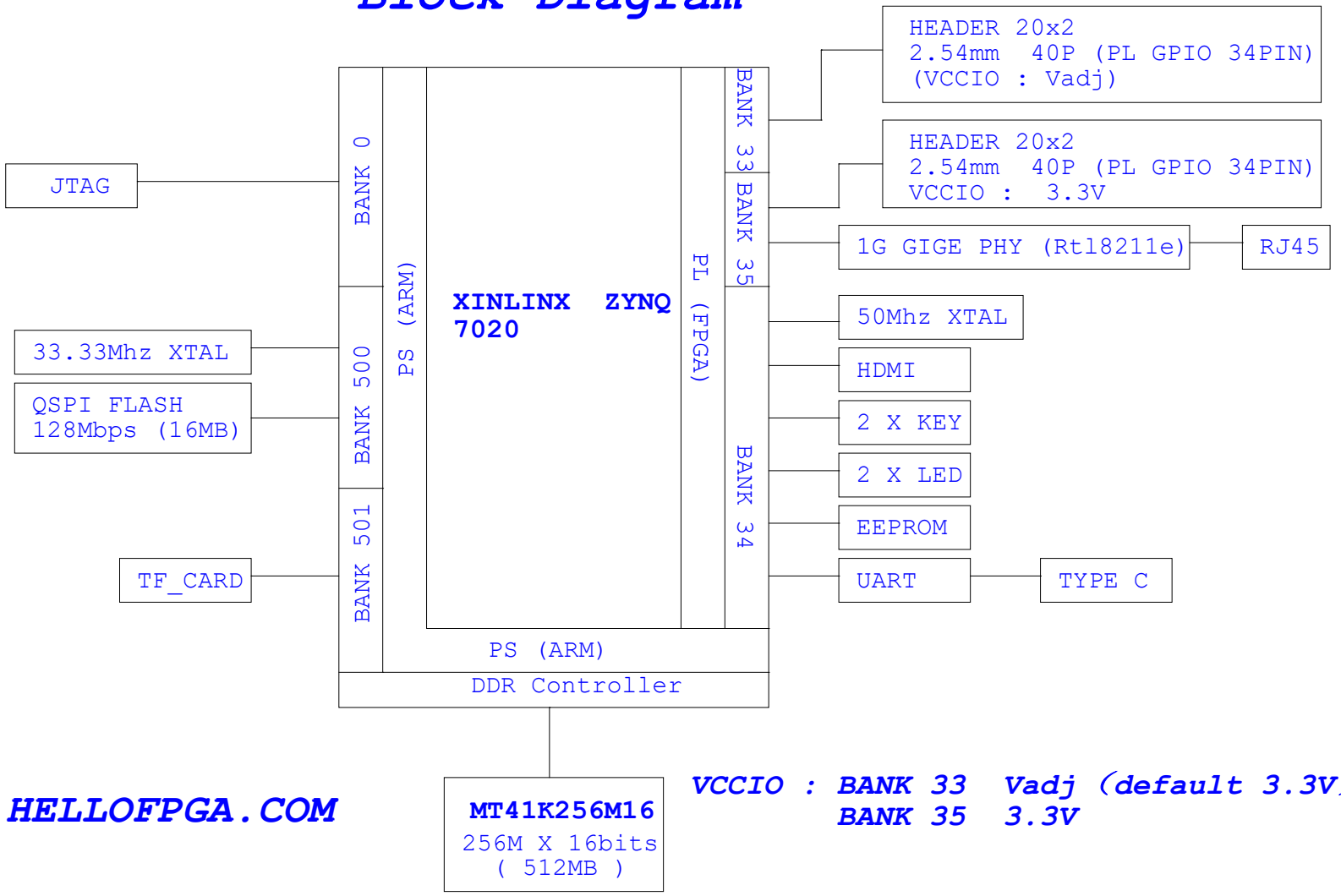
Smart ZYNQ SL VER: 1.2
Block Diagram



HELLOFPGA.COM

VCCIO : BANK 33 Vadj (default 3.3V)
BANK 35 3.3V

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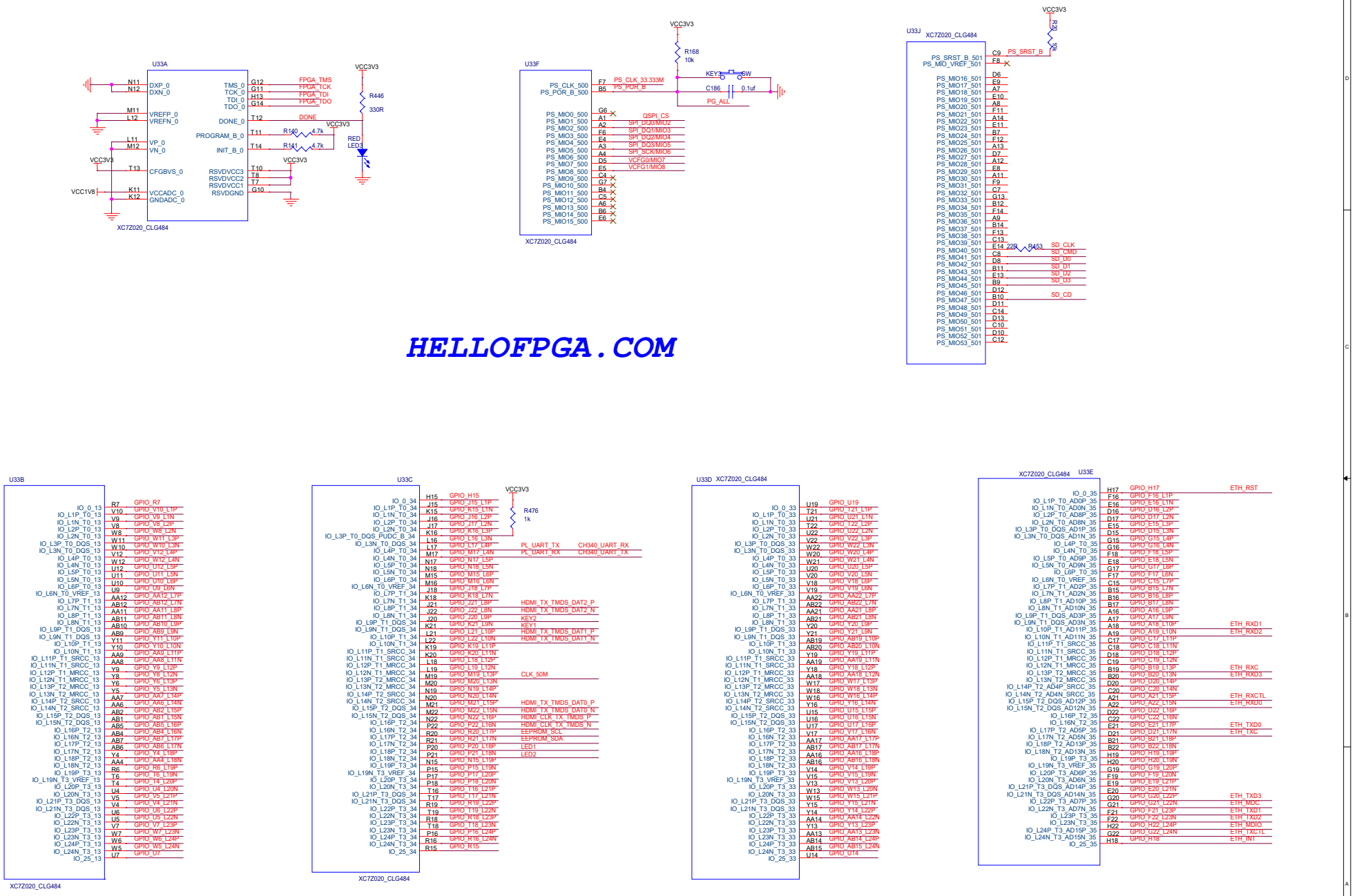
U33A
XC7Z020_CLG484
VCC3V3
R446
330R
RED
LED3
DONE
R140 4.7k
R141 4.7k
FPGA_TMS
FPGA_TCK
FPGA_TDI
FPGA_TDO
U33F
XC7Z020_CLG484
R168
10k
KEY3
SW
C186
0.1uf
PG_ALL
PS_CLK_33.333M
QSPI_CS
SPI_DQ0/MIO2
SPI_DQ1/MIO3
SPI_DQ2/MIO4
SPI_DQ3/MIO5
SPI_SCK/MIO6
VCFG0/MIO7
VCFG1/MIO8
U33J
XC7Z020_CLG484
R2k
40k
PS_SRST_B
R453 22R
SD_CLK
SD_CMD
SD_D0
SD_D1
SD_D2
SD_D3
SD_CD
HELLOFPGA.COM
U33B
XC7Z020_CLG484
U33C
XC7Z020_CLG484
R476
1k
PL_UART_TX
PL_UART_RX
CH340_UART_RX
CH340_UART_TX
HDMI_TX_TMDS_DAT2_P
HDMI_TX_TMDS_DAT2_N
KEY2
KEY1
HDMI_TX_TMDS_DAT1_P
HDMI_TX_TMDS_DAT1_N
CLK_50M
HDMI_TX_TMDS_DAT0_P
HDMI_TX_TMDS_DAT0_N
HDMI_CLK_TX_TMDS_P
HDMI_CLK_TX_TMDS_N
EEPROM_SCL
EEPROM_SDA
LED1
LED2
U33D XC7Z020_CLG484
U33E
XC7Z020_CLG484
ETH_RST
ETH_RXD1
ETH_RXD2
ETH_RXC
ETH_RXD3
ETH_RXCTL
ETH_RXD0
ETH_TXC
ETH_TXD0
ETH_TXD3
ETH_MDC
ETH_TXD1
ETH_TXD2
ETH_MDIO
ETH_TXCTL
ETH_INT
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DDR3_VREF2
DDR3_VREF2
U33G
PS_DDR_VREF1_502
PS_DDR_VREF0_502
PS_DDR_A14_502
PS_DDR_A13_502
PS_DDR_A12_502
PS_DDR_A11_502
PS_DDR_A10_502
PS_DDR_A9_502
PS_DDR_A8_502
PS_DDR_A7_502
PS_DDR_A6_502
PS_DDR_A5_502
PS_DDR_A4_502
PS_DDR_A3_502
PS_DDR_A2_502
PS_DDR_A1_502
PS_DDR_A0_502
PS_DDR_BA2_502
PS_DDR_BA1_502
PS_DDR_BA0_502
PS_DDR_DRST_B_502
PS_DDR_RAS_B_502
PS_DDR_CAS_B_502
PS_DDR_CS_B_502
PS_DDR_WE_B_502
PS_DDR_CKE_502
PS_DDR_CKP_502
PS_DDR_CKN_502
PS_DDR_ODT_502
PS_DDR_VRP_502
PS_DDR_VRN_502
PS_DDR_DQ31_502
PS_DDR_DQ30_502
PS_DDR_DQ29_502
PS_DDR_DQ28_502
PS_DDR_DQ27_502
PS_DDR_DQ26_502
PS_DDR_DQ25_502
PS_DDR_DQ24_502
PS_DDR_DQ23_502
PS_DDR_DQ22_502
PS_DDR_DQ21_502
PS_DDR_DQ20_502
PS_DDR_DQ19_502
PS_DDR_DQ18_502
PS_DDR_DQ17_502
PS_DDR_DQ16_502
PS_DDR_DQ15_502
PS_DDR_DQ14_502
PS_DDR_DQ13_502
PS_DDR_DQ12_502
PS_DDR_DQ11_502
PS_DDR_DQ10_502
PS_DDR_DQ9_502
PS_DDR_DQ8_502
PS_DDR_DQ7_502
PS_DDR_DQ6_502
PS_DDR_DQ5_502
PS_DDR_DQ4_502
PS_DDR_DQ3_502
PS_DDR_DQ2_502
PS_DDR_DQ1_502
PS_DDR_DQ0_502
PS_DDR_DM3_502
PS_DDR_DM2_502
PS_DDR_DM1_502
PS_DDR_DM0_502
PS_DDR_DQS_P3_502
PS_DDR_DQS_N3_502
PS_DDR_DQS_P2_502
PS_DDR_DQS_N2_502
PS_DDR_DQS_P1_502
PS_DDR_DQS_N1_502
PS_DDR_DQS_P0_502
PS_DDR_DQS_N0_502
XC7Z020_CLG484
MEM_ADD14
MEM_ADD13
MEM_ADD12
MEM_ADD11
MEM_ADD10
MEM_ADD9
MEM_ADD8
MEM_ADD7
MEM_ADD6
MEM_ADD5
MEM_ADD4
MEM_ADD3
MEM_ADD2
MEM_ADD1
MEM_ADD0
MEM_BANK2
MEM_BANK1
MEM_BANK0
MEM_RESET#
MEM_RAS#
MEM_CAS#
MEM_MA0_CS_L0
MEM_WE#
MEM_MA0_CKE0
MEM_CLK0_P
MEM_CLK0_N
R10
80.6r
MEM_MA0_ODT0
R13
R14
80.6r
80.6r
VCC1V5
DDR3_D15
DDR3_D14
DDR3_D13
DDR3_D12
DDR3_D11
DDR3_D10
DDR3_D9
DDR3_D8
DDR3_D7
DDR3_D6
DDR3_D5
DDR3_D4
DDR3_D3
DDR3_D2
DDR3_D1
DDR3_D0
MEM_DM1
MEM_DM0
MEM_DQS1_P
MEM_DQS1_N
MEM_DQS0_P
MEM_DQS0_N
J1
MEM_ADD0
MEM_ADD1
MEM_ADD2
MEM_ADD3
MEM_ADD4
MEM_ADD5
MEM_ADD6
MEM_ADD7
MEM_ADD8
MEM_ADD9
MEM_ADD10
MEM_ADD11
MEM_ADD12
MEM_ADD13
MEM_ADD14
MEM_BANK0
MEM_BANK1
MEM_BANK2
MEM_RAS#
MEM_CAS#
MEM_WE#
MEM_CLK0_P
MEM_CLK0_N
MEM_DQS0_P
MEM_DQS0_N
MEM_DQS1_P
MEM_DQS1_N
MEM_DM0
MEM_DM1
MEM_MA0_CKE0
MEM_MA0_CS_L0
MEM_MA0_ODT0
MEM_RESET#
DDR3_VREF
R12
4.7k
R15
240R
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10/AP
A11
A12/BC_L
A13
A14/NC
A15/NC
BA0
BA1
BA2
RAS_L
CAS_L
WE_L
CK
CK_L
LDQS
LDQS_L
UDQS
UDQS_L
LDM
UDM
CKE0
CKE1/NC
CS0_L
CS1_L/NC
ODT0
ODT1/NC
RESET_L
VREFCA
VREFDQ
ZQ0
ZQ1/NC
VSS0
VSS1
VSS2
VSS3
VSS4
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
VDD0
VDD1
VDD2
VDD3
VDD4
VDD5
VDD6
VDD7
VDD8
VDDQ0
VDDQ1
VDDQ2
VDDQ3
VDDQ4
VDDQ5
VDDQ6
VDDQ7
VDDQ8
VSSQ0
VSSQ1
VSSQ2
VSSQ3
VSSQ4
VSSQ5
VSSQ6
VSSQ7
VSSQ8
VSS5
VSS6
VSS7
VSS8
VSS9
VSS10
VSS11
MT41K256M16TW-107
DDR3_D0
DDR3_D7
DDR3_D1
DDR3_D6
DDR3_D3
DDR3_D5
DDR3_D2
DDR3_D4
DDR3_D13
DDR3_D11
DDR3_D14
DDR3_D10
DDR3_D9
DDR3_D12
DDR3_D8
DDR3_D15
VCC1V5
C2
C3
C4
C5
C6
C7
C150
10uf
1uf
1uf
0.1uf
0.1uf
0.1uf
10nf
VCC1V5
C12
C13
C14
C15
C16
C17
0.1uf
0.1uf
0.1uf
0.1uf
0.1uf
10nf
VCC1V5
R16
1k
R18
1k
C151
C159
0.1uf
10nf
C21
C22
0.1uf
10nf
DDR3_VREF
VCC1V5
R144
1k
R145
1k
C155
0.1uf
C156
C160
0.1uf
0.1uf
DDR3_VREF2
DDR PART
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<Doc>
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<1.2>
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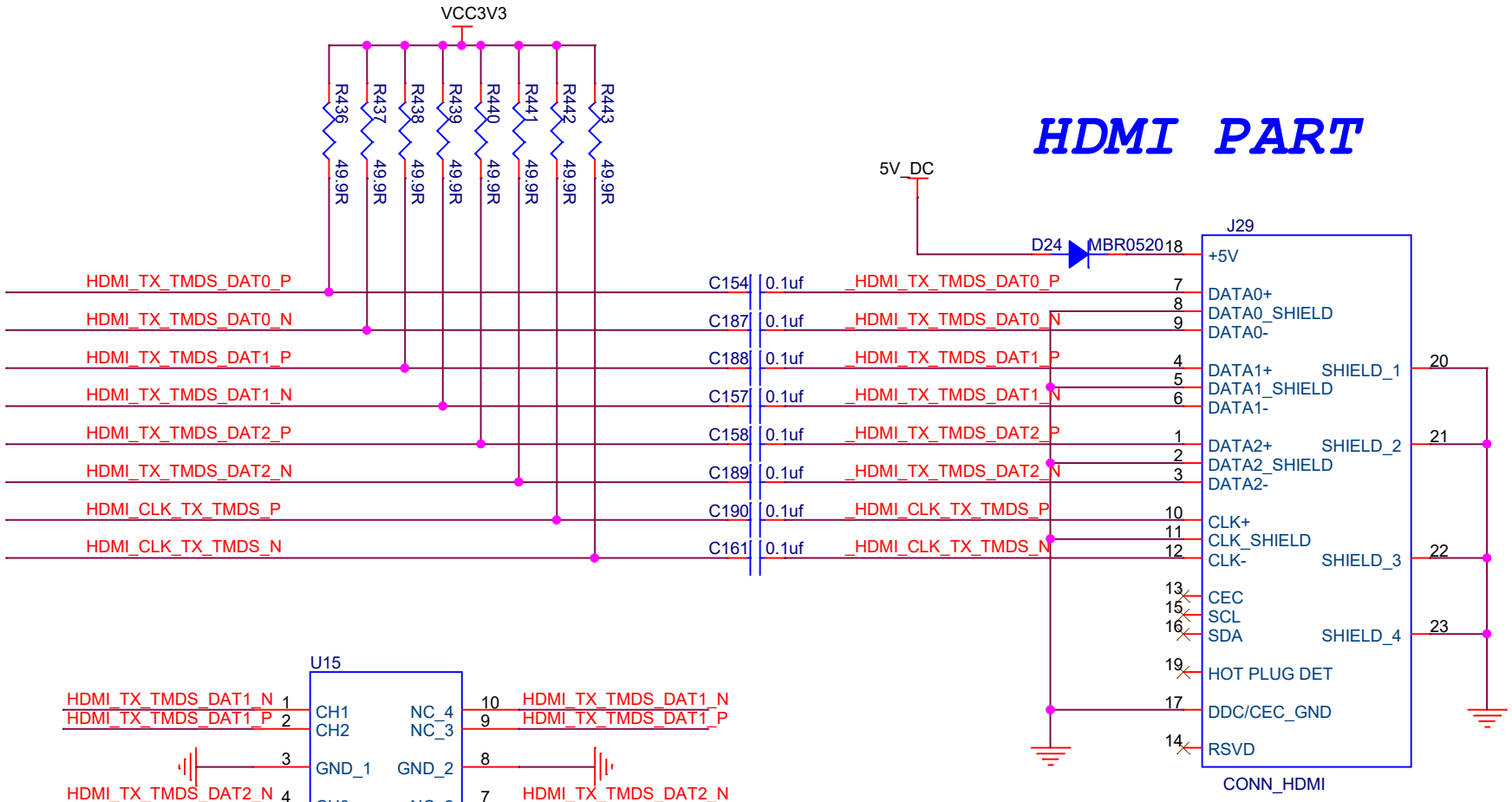

Title	HELLOFPGA.COM	
Size A	Document Number <Doc>	Rev <1.2>
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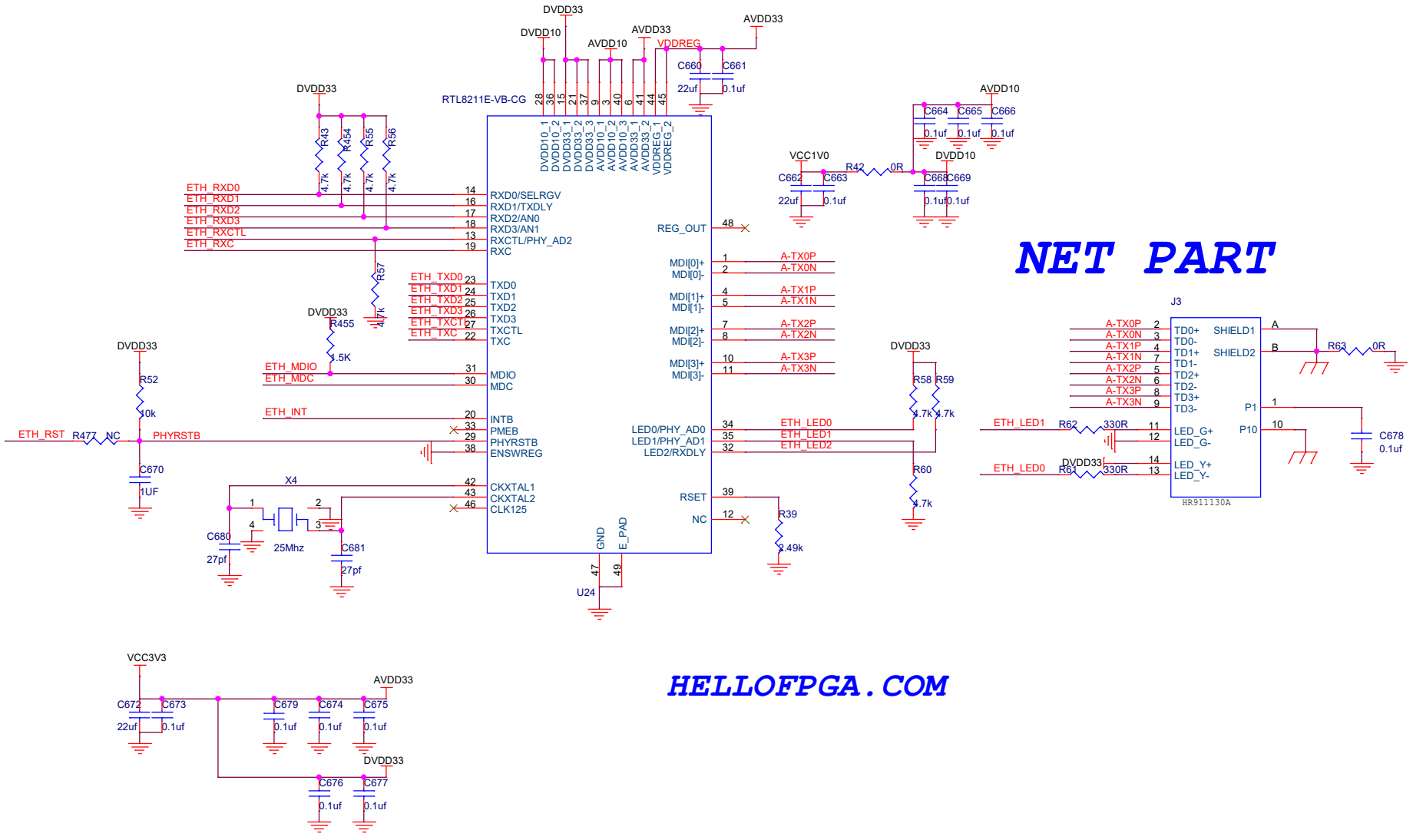

Title	HELLOFPGA.COM	
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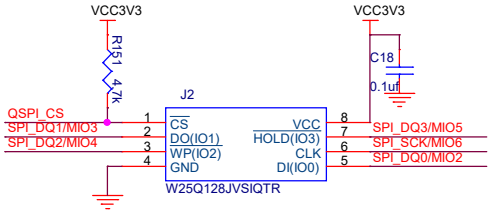
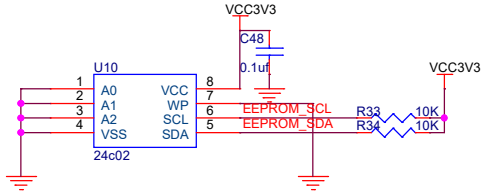
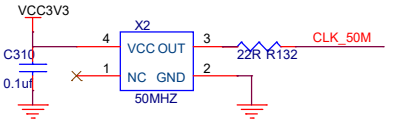
QSPI FLASH



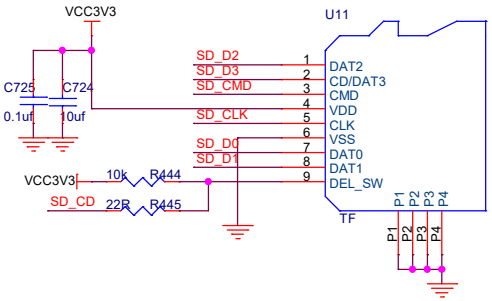
EEPROM



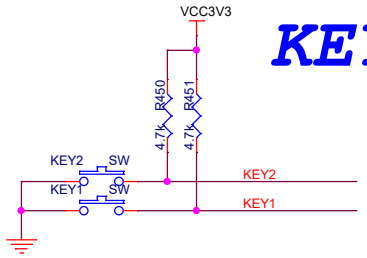
PL CLK



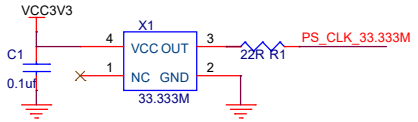
TF CARD



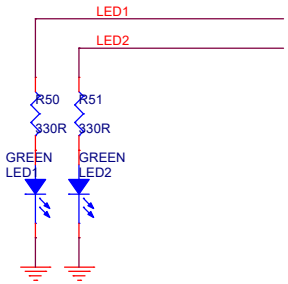
KEY



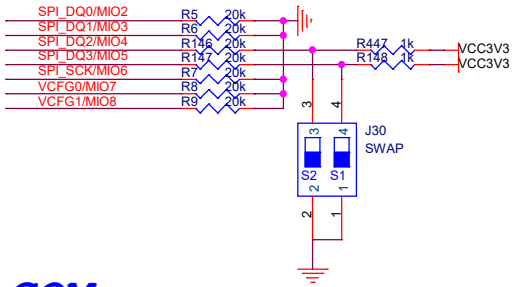
PS CLK



LED



BOOT



BOOT

BOOT	S1	S2
JTAG	●	●
QSPI	○	●
SD	○	○

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Title: HELLOFPGA.COM		
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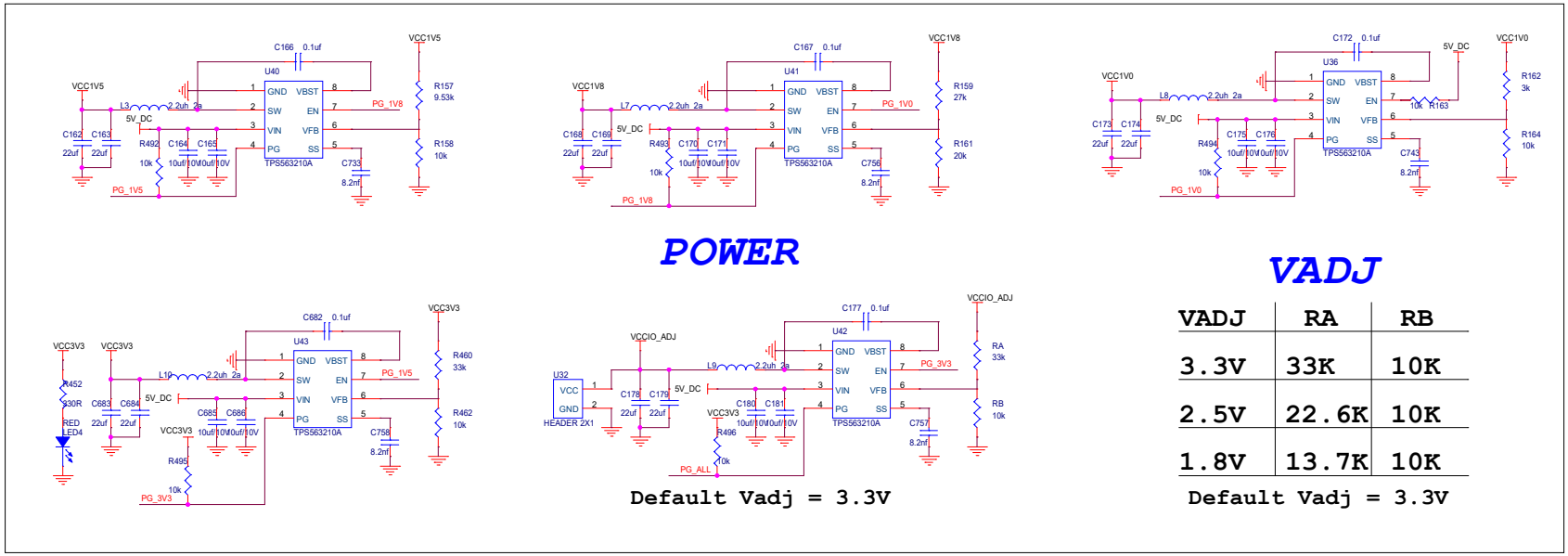

VADJ	RA	RB
3.3V	33K	10K
2.5V	22.6K	10K
1.8V	13.7K	10K

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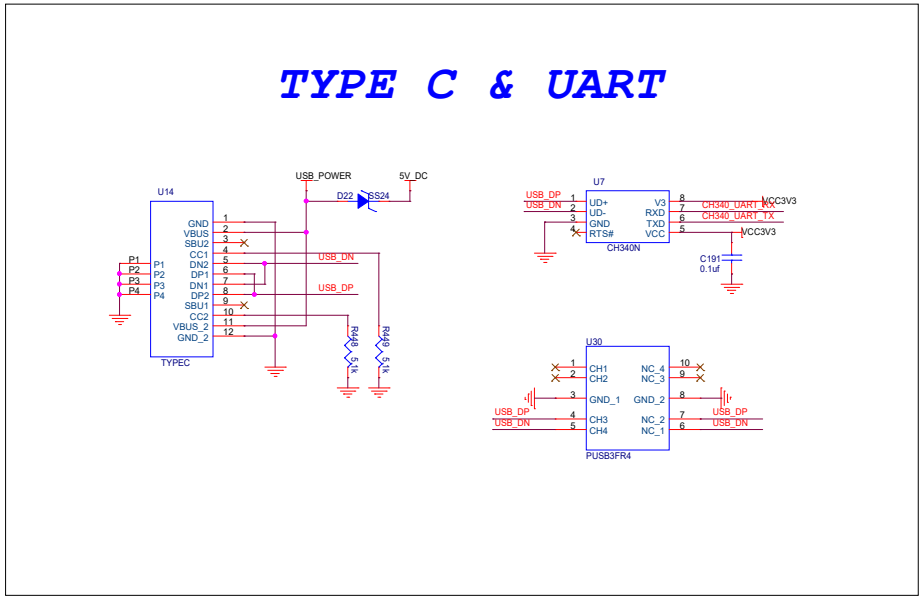

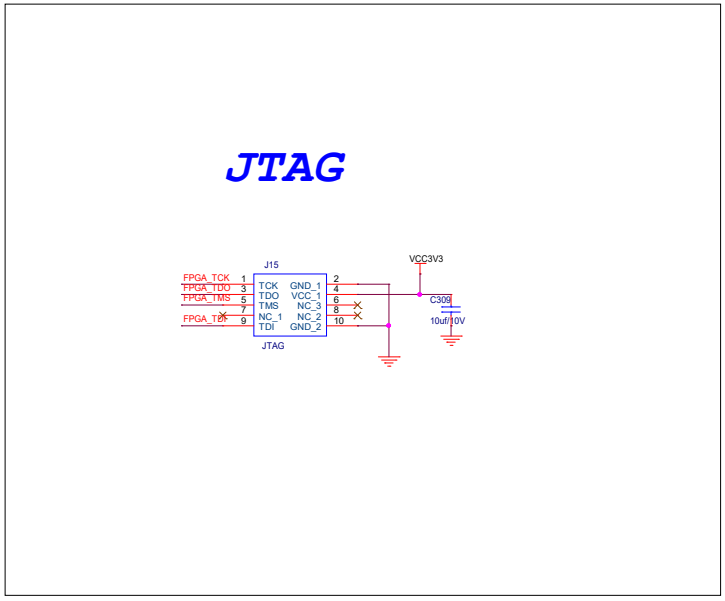

Title	HELLOFPGA.COM	
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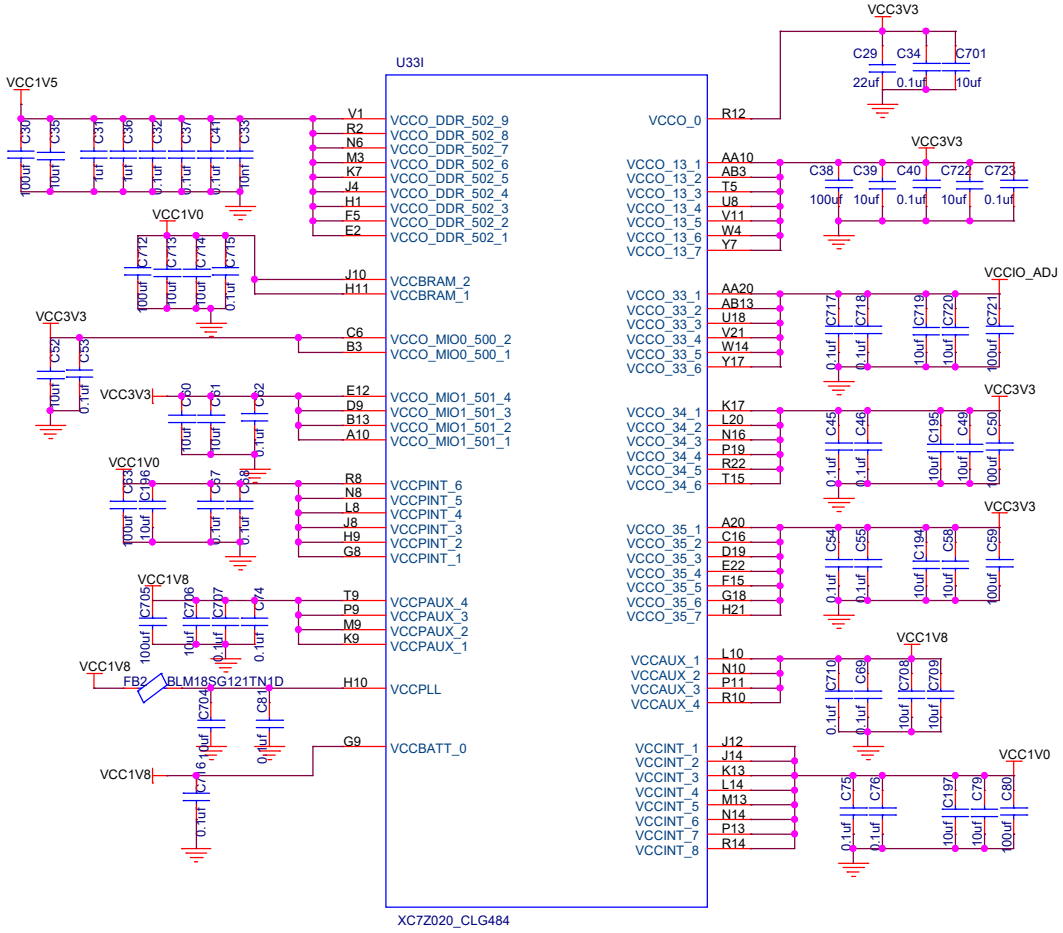

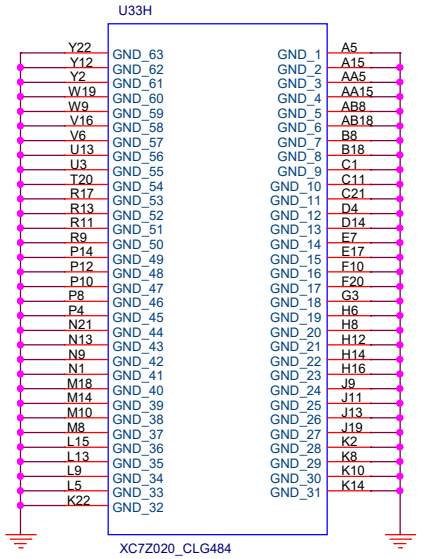

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Title: HELLOFPGA.COM		
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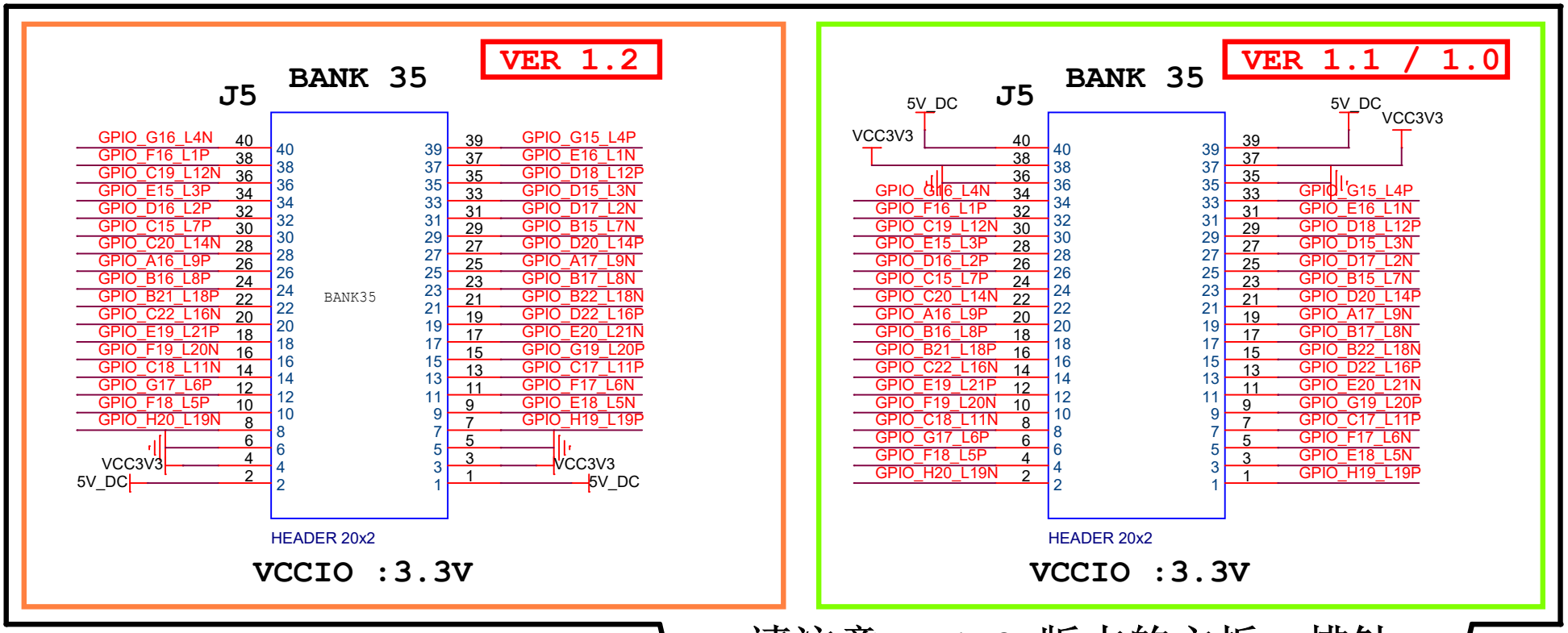
VER 1.2
J5
BANK 35
GPIO_G16_L4N 40
GPIO_F16_L1P 38
GPIO_C19_L12N 36
GPIO_E15_L3P 34
GPIO_D16_L2P 32
GPIO_C15_L7P 30
GPIO_C20_L14N 28
GPIO_A16_L9P 26
GPIO_B16_L8P 24
GPIO_B21_L18P 22
GPIO_C22_L16N 20
GPIO_E19_L21P 18
GPIO_F19_L20N 16
GPIO_C18_L11N 14
GPIO_G17_L6P 12
GPIO_F18_L5P 10
GPIO_H20_L19N 8
6
VCC3V3 4
5V_DC 2
BANK35
39 GPIO_G15_L4P
37 GPIO_E16_L1N
35 GPIO_D18_L12P
33 GPIO_D15_L3N
31 GPIO_D17_L2N
29 GPIO_B15_L7N
27 GPIO_D20_L14P
25 GPIO_A17_L9N
23 GPIO_B17_L8N
21 GPIO_B22_L18N
19 GPIO_D22_L16P
17 GPIO_E20_L21N
15 GPIO_G19_L20P
13 GPIO_C17_L11P
11 GPIO_F17_L6N
9 GPIO_E18_L5N
7 GPIO_H19_L19P
5
3 VCC3V3
1 5V_DC
HEADER 20x2
VCCIO :3.3V
VER 1.1 / 1.0
J5
BANK 35
5V_DC
VCC3V3
GPIO_C16_L4N 34
GPIO_F16_L1P 32
GPIO_C19_L12N 30
GPIO_E15_L3P 28
GPIO_D16_L2P 26
GPIO_C15_L7P 24
GPIO_C20_L14N 22
GPIO_A16_L9P 20
GPIO_B16_L8P 18
GPIO_B21_L18P 16
GPIO_C22_L16N 14
GPIO_E19_L21P 12
GPIO_F19_L20N 10
GPIO_C18_L11N 8
GPIO_G17_L6P 6
GPIO_F18_L5P 4
GPIO_H20_L19N 2
5V_DC
VCC3V3
39
37
35
33 GPIO_G15_L4P
31 GPIO_E16_L1N
29 GPIO_D18_L12P
27 GPIO_D15_L3N
25 GPIO_D17_L2N
23 GPIO_B15_L7N
21 GPIO_D20_L14P
19 GPIO_A17_L9N
17 GPIO_B17_L8N
15 GPIO_B22_L18N
13 GPIO_D22_L16P
11 GPIO_E20_L21N
9 GPIO_G19_L20P
7 GPIO_C17_L11P
5 GPIO_F17_L6N
3 GPIO_E18_L5N
1 GPIO_H19_L19P
HEADER 20x2
VCCIO :3.3V
J6
BANK 33
5V_DC 40
VCC3V3 38
36
GPIO_V14_L19P 34
GPIO_AA14_L22N 32
GPIO_Y16_L14N 30
GPIO_AB17_L17N 28
GPIO_W17_L13P 26
GPIO_W13_L20N 24
GPIO_AA13_L23N 22
GPIO_AB15_L24N 20
GPIO_AA18_L12N 18
GPIO_AA16_L18P 16
GPIO_Y19_L11P 14
GPIO_AB20_L10N 12
GPIO_AA21_L8P 10
GPIO_AA22_L7P 8
GPIO_Y20_L9P 6
GPIO_V22_L3P 4
GPIO_T22_L2P 2
BANK33
39 5V_DC
37 VCC3V3
35
33 GPIO_V15_L19N
31 GPIO_Y14_L22P
29 GPIO_W16_L14P
27 GPIO_AA17_L17P
25 GPIO_W18_L13N
23 GPIO_V13_L20P
21 GPIO_Y13_L23P
19 GPIO_AB14_L24P
17 GPIO_Y18_L12P
15 GPIO_AB16_L18N
13 GPIO_AA19_L11N
11 GPIO_AB19_L10P
9 GPIO_AB21_L8N
7 GPIO_AB22_L7N
5 GPIO_Y21_L9N
3 GPIO_W22_L3N
1 GPIO_U22_L2N
HEADER 20x2
VCCIO :VADJ
Default Vadj = 3.3V
请注意：V1.2 版本的主板J5排针部分和V1.1/V1.0版本并不兼容
Please note: Version 1.2 J5 pinout is not compatible with versions 1.1/1.0.
版本信息标注在主板的丝印上
Please check the version information indicated on the silk-screen markings of the motherboard
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UART

ZYNQ_TX	L17
ZYNQ_RX	M17

EEPROM

SCL	R20
SDA	R21

50M CLOCK

CLK	M19

KEY & LED

KEY1	K21
KEY2	J20
LED1	P20
LED2	P21

HDMI

CLK	N22
D0	M21
D1	L21
D2	J21

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GigE phy

ETH TD0	E21
ETH TD1	F21
ETH TD2	F22
ETH TD3	G20
ETH TX_CTL	G22
ETH TXC	D21
ETH RD0	A22
ETH RD1	A18
ETH RD2	A19
ETH RD3	B20
ETH RX_CTL	A21
ETH RXC	B19
ETH MDIO	H22
ETH MDC	G21
ETH INT	H18

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Smart ZYNQ SL board
Pin Constraint Definition Reference

```
create_clock -period 20 -name clk_50 [get_ports clk_50]
set_property -dict {PACKAGE_PIN M19 IOSTANDARD LVCMOS33} [get_ports clk_50]

set_property -dict {PACKAGE_PIN M17 IOSTANDARD LVCMOS33} [get_ports uart_rxd]
set_property -dict {PACKAGE_PIN L17 IOSTANDARD LVCMOS33} [get_ports uart_txd]

set_property -dict {PACKAGE_PIN P20 IOSTANDARD LVCMOS33} [get_ports LED1]
set_property -dict {PACKAGE_PIN P21 IOSTANDARD LVCMOS33} [get_ports LED2]
set_property -dict {PACKAGE_PIN K21 IOSTANDARD LVCMOS33} [get_ports KEY1]
set_property -dict {PACKAGE_PIN J20 IOSTANDARD LVCMOS33} [get_ports KEY2]

set_property -dict {PACKAGE_PIN R20 IOSTANDARD LVCMOS33} [get_ports EEPROM_SCL]
set_property -dict {PACKAGE_PIN R21 IOSTANDARD LVCMOS33} [get_ports EEPROM_SDA]

# HDMI (DVI) outputs
set_property PACKAGE_PIN J21 [get_ports {hdmi_d_p[2]}]
set_property PACKAGE_PIN L21 [get_ports {hdmi_d_p[1]}]
set_property PACKAGE_PIN M21 [get_ports {hdmi_d_p[0]}]
set_property PACKAGE_PIN N22 [get_ports hdmi_clk_p]

# RGMII PHY
create_clock -period 8 -name RGMII_rxc [get_ports RGMII_rxc]
set_property -dict {PACKAGE_PIN G21 IOSTANDARD LVCMOS33} [get_ports MDIO_PHY_mdc]
set_property -dict {PACKAGE_PIN H22 IOSTANDARD LVCMOS33} [get_ports MDIO_PHY_mdio_io]
set_property -dict {PACKAGE_PIN A22 IOSTANDARD LVCMOS33} [get_ports {RGMII_rd[0]}]
set_property -dict {PACKAGE_PIN A18 IOSTANDARD LVCMOS33} [get_ports {RGMII_rd[1]}]
set_property -dict {PACKAGE_PIN A19 IOSTANDARD LVCMOS33} [get_ports {RGMII_rd[2]}]
set_property -dict {PACKAGE_PIN B20 IOSTANDARD LVCMOS33} [get_ports {RGMII_rd[3]}]
set_property -dict {PACKAGE_PIN A21 IOSTANDARD LVCMOS33} [get_ports RGMII_rx_ctl]
set_property -dict {PACKAGE_PIN B19 IOSTANDARD LVCMOS33} [get_ports RGMII_rxc]
set_property -dict {PACKAGE_PIN E21 IOSTANDARD LVCMOS33} [get_ports {RGMII_td[0]}]
set_property -dict {PACKAGE_PIN F21 IOSTANDARD LVCMOS33} [get_ports {RGMII_td[1]}]
set_property -dict {PACKAGE_PIN F22 IOSTANDARD LVCMOS33} [get_ports {RGMII_td[2]}]
set_property -dict {PACKAGE_PIN G20 IOSTANDARD LVCMOS33} [get_ports {RGMII_td[3]}]
set_property -dict {PACKAGE_PIN G22 IOSTANDARD LVCMOS33} [get_ports RGMII_tx_ctl]
set_property -dict {PACKAGE_PIN D21 IOSTANDARD LVCMOS33} [get_ports RGMII_txc]
set_property SLEW FAST [get_ports {RGMII_td[0]}]
set_property SLEW FAST [get_ports {RGMII_td[1]}]
set_property SLEW FAST [get_ports {RGMII_td[2]}]
set_property SLEW FAST [get_ports {RGMII_td[3]}]
set_property SLEW FAST [get_ports RGMII_tx_ctl]
set_property SLEW FAST [get_ports RGMII_txc]
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## J5 on board (BANK35 V3V3)
# Set voltage level for banks35 (match with jumper setting on board)
set_property IOSTANDARD LVCMOS33 [get_ports {J5[*]}]
set_property PACKAGE_PIN H19 [get_ports {J5[0]}];    #IO_B35_LP19
set_property PACKAGE_PIN H20 [get_ports {J5[1]}];    #IO_B35_LN19
set_property PACKAGE_PIN E18 [get_ports {J5[2]}];    #IO_B35_LN5
set_property PACKAGE_PIN F18 [get_ports {J5[3]}];    #IO_B35_LP5
set_property PACKAGE_PIN F17 [get_ports {J5[4]}];    #IO_B35_LN6
set_property PACKAGE_PIN G17 [get_ports {J5[5]}];    #IO_B35_LP6
set_property PACKAGE_PIN C17 [get_ports {J5[6]}];    #IO_B35_LP11
set_property PACKAGE_PIN C18 [get_ports {J5[7]}];    #IO_B35_LN11
set_property PACKAGE_PIN G19 [get_ports {J5[8]}];    #IO_B35_LP20
set_property PACKAGE_PIN F19 [get_ports {J5[9]}];    #JIO_B35_LN20
set_property PACKAGE_PIN E20 [get_ports {J5[10]}];   #IO_B35_LN21
set_property PACKAGE_PIN E19 [get_ports {J5[11]}];   #IO_B35_LP21
set_property PACKAGE_PIN D22 [get_ports {J5[12]}];   #IO_B35_LP16
set_property PACKAGE_PIN C22 [get_ports {J5[13]}];   #IO_B35_LN16
set_property PACKAGE_PIN B22 [get_ports {J5[14]}];   #IO_B35_LN18
set_property PACKAGE_PIN B21 [get_ports {J5[15]}];   #IO_B35_LP18
set_property PACKAGE_PIN B17 [get_ports {J5[16]}];   #IO_B35_LN8
set_property PACKAGE_PIN B16 [get_ports {J5[17]}];   #IO_B35_LP8
set_property PACKAGE_PIN A17 [get_ports {J5[18]}];   #IO_B35_LN9
set_property PACKAGE_PIN A16 [get_ports {J5[19]}];   #IO_B35_LP9
set_property PACKAGE_PIN D20 [get_ports {J5[20]}];   #IO_B35_LP14
set_property PACKAGE_PIN C20 [get_ports {J5[21]}];   #IO_B35_LN14
set_property PACKAGE_PIN B15 [get_ports {J5[22]}];   #IO_B35_LN7
set_property PACKAGE_PIN C15 [get_ports {J5[23]}];   #IO_B35_LP7
set_property PACKAGE_PIN D17 [get_ports {J5[24]}];   #IO_B35_LN2
set_property PACKAGE_PIN D16 [get_ports {J5[25]}];   #IO_B35_LP2
set_property PACKAGE_PIN D15 [get_ports {J5[26]}];   #IO_B35_LN3
set_property PACKAGE_PIN E15 [get_ports {J5[27]}];   #IO_B35_LP3
set_property PACKAGE_PIN D18 [get_ports {J5[28]}];   #IO_B35_LP12
set_property PACKAGE_PIN C19 [get_ports {J5[29]}];   #IO_B35_LN12
set_property PACKAGE_PIN E16 [get_ports {J5[30]}];   #IO_B35_LN1
set_property PACKAGE_PIN F16 [get_ports {J5[31]}];   #IO_B35_LP1
set_property PACKAGE_PIN G15 [get_ports {J5[32]}];   #IO_B35_LP4
set_property PACKAGE_PIN G16 [get_ports {J5[33]}];   #IO_B35_LN4


## J6 on board (BANK33 VADJ)
# Set voltage level for banks 33 (match with jumper setting on board)
set_property IOSTANDARD LVCMOS33 [get_ports {J6[*]}]
set_property PACKAGE_PIN U22  [get_ports {J6[0]}];   #J6/1  = IO_B33_LN2
set_property PACKAGE_PIN T22  [get_ports {J6[1]}];   #J6/2  = IO_B33_LP2
set_property PACKAGE_PIN W22  [get_ports {J6[2]}];   #J6/3  = IO_B33_LN3
set_property PACKAGE_PIN V22  [get_ports {J6[3]}];   #J6/4  = IO_B33_LP3
set_property PACKAGE_PIN Y21  [get_ports {J6[4]}];   #J6/5  = IO_B33_LN9
set_property PACKAGE_PIN Y20  [get_ports {J6[5]}];   #J6/6  = IO_B33_LP9
set_property PACKAGE_PIN AB22 [get_ports {J6[6]}];   #J6/7  = IO_B33_LN7
set_property PACKAGE_PIN AA22 [get_ports {J6[7]}];   #J6/8  = IO_B33_LP7
set_property PACKAGE_PIN AB21 [get_ports {J6[8]}];   #J6/9  = IO_B33_LN8
set_property PACKAGE_PIN AA21 [get_ports {J6[9]}];   #J6/10 = IO_B33_LP8
set_property PACKAGE_PIN AB19 [get_ports {J6[10]}];  #J6/11 = IO_B33_LP10
set_property PACKAGE_PIN AB20 [get_ports {J6[11]}];  #J6/12 = IO_B33_LN10
set_property PACKAGE_PIN AA19 [get_ports {J6[12]}];  #J6/13 = IO_B33_LN11
set_property PACKAGE_PIN Y19  [get_ports {J6[13]}];  #J6/14 = IO_B33_LP11
set_property PACKAGE_PIN AB16 [get_ports {J6[14]}];  #J6/15 = IO_B33_LN18
set_property PACKAGE_PIN AA16 [get_ports {J6[15]}];  #J6/16 = IO_B33_LP18
set_property PACKAGE_PIN Y18  [get_ports {J6[16]}];  #J6/17 = IO_B33_LP12
set_property PACKAGE_PIN AA18 [get_ports {J6[17]}];  #J6/18 = IO_B33_LN12
set_property PACKAGE_PIN AB14 [get_ports {J6[18]}];  #J6/19 = IO_B33_LP24
set_property PACKAGE_PIN AB15 [get_ports {J6[19]}];  #J6/20 = IO_B33_LN24
set_property PACKAGE_PIN Y13  [get_ports {J6[20]}];  #J6/21 = IO_B33_LP23
set_property PACKAGE_PIN AA13 [get_ports {J6[21]}];  #J6/22 = IO_B33_LN23
set_property PACKAGE_PIN V13  [get_ports {J6[22]}];  #J6/23 = IO_B33_LP20
set_property PACKAGE_PIN W13  [get_ports {J6[23]}];  #J6/24 = IO_B33_LN20
set_property PACKAGE_PIN W18  [get_ports {J6[24]}];  #J6/25 = IO_B33_LN13
set_property PACKAGE_PIN W17  [get_ports {J6[25]}];  #J6/26 = IO_B33_LP13
set_property PACKAGE_PIN AA17 [get_ports {J6[26]}];  #J6/27 = IO_B33_LP17
set_property PACKAGE_PIN AB17 [get_ports {J6[27]}];  #J6/28 = IO_B33_LN17
set_property PACKAGE_PIN W16  [get_ports {J6[28]}];  #J6/29 = IO_B33_LP14
set_property PACKAGE_PIN Y16  [get_ports {J6[29]}];  #J6/30 = IO_B33_LN14
set_property PACKAGE_PIN Y14  [get_ports {J6[30]}];  #J6/31 = IO_B33_LP22
set_property PACKAGE_PIN AA14 [get_ports {J6[31]}];  #J6/32 = IO_B33_LN22
set_property PACKAGE_PIN V15  [get_ports {J6[32]}];  #J6/33 = IO_B33_LN19
set_property PACKAGE_PIN V14  [get_ports {J6[33]}];  #J6/34 = IO_B33_LP19
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