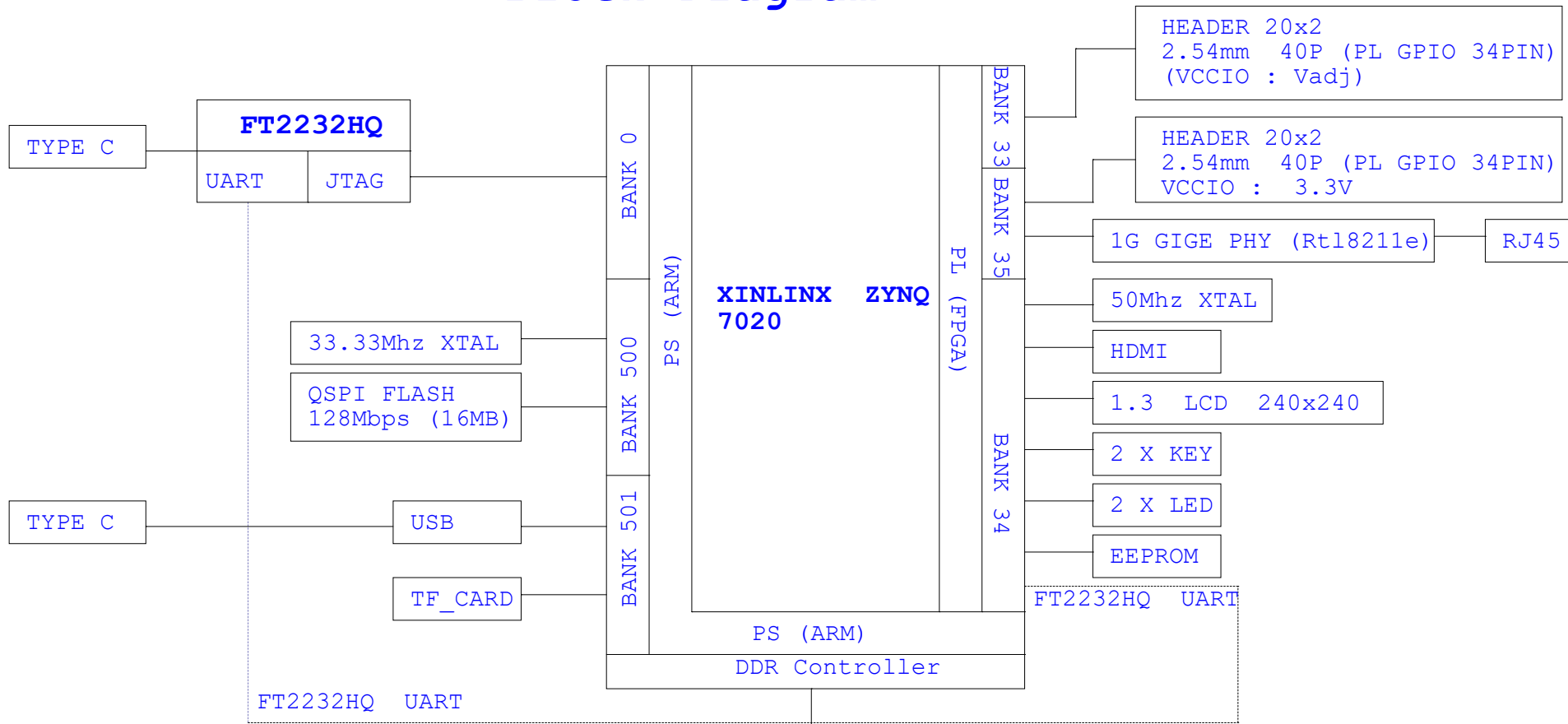


Smart ZYNQ SP2 V1.3 Block Diagram

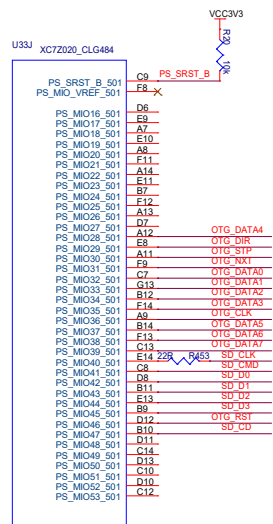
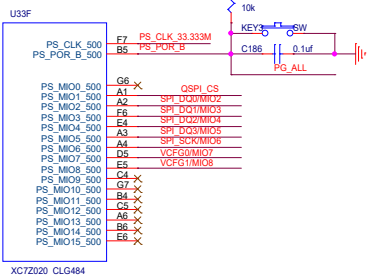
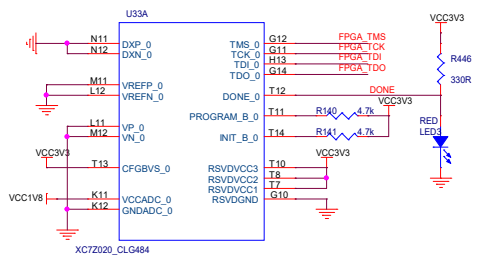
此原理图同样适用于v1.0 v1.1版本硬件电路
This schematic is also applicable to the V1.0 and V1.1 version hardware circuits.



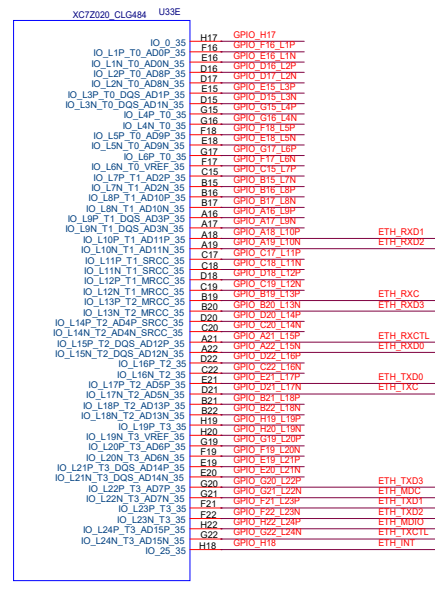
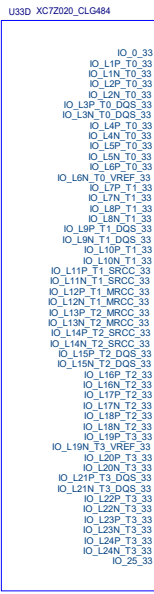
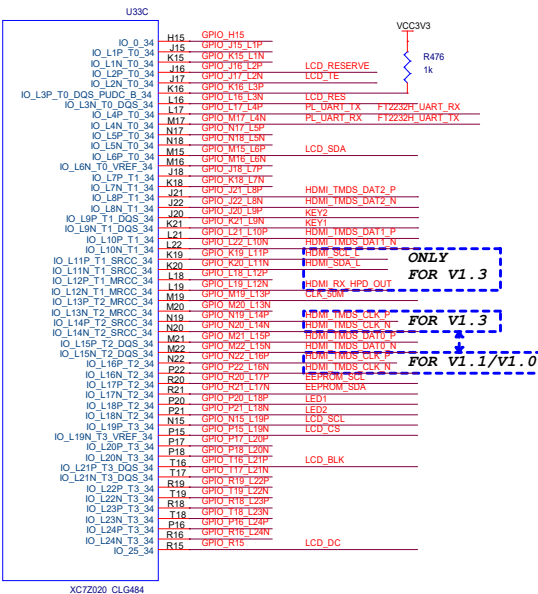
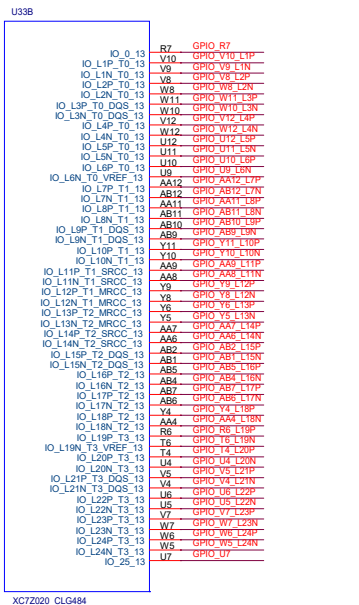
VCCIO : BANK 33 Vadj (default 3.3V)
BANK 34 3.3V
BANK 35 3.3V

MT41K256M16
256M X 16bits
(512MB)

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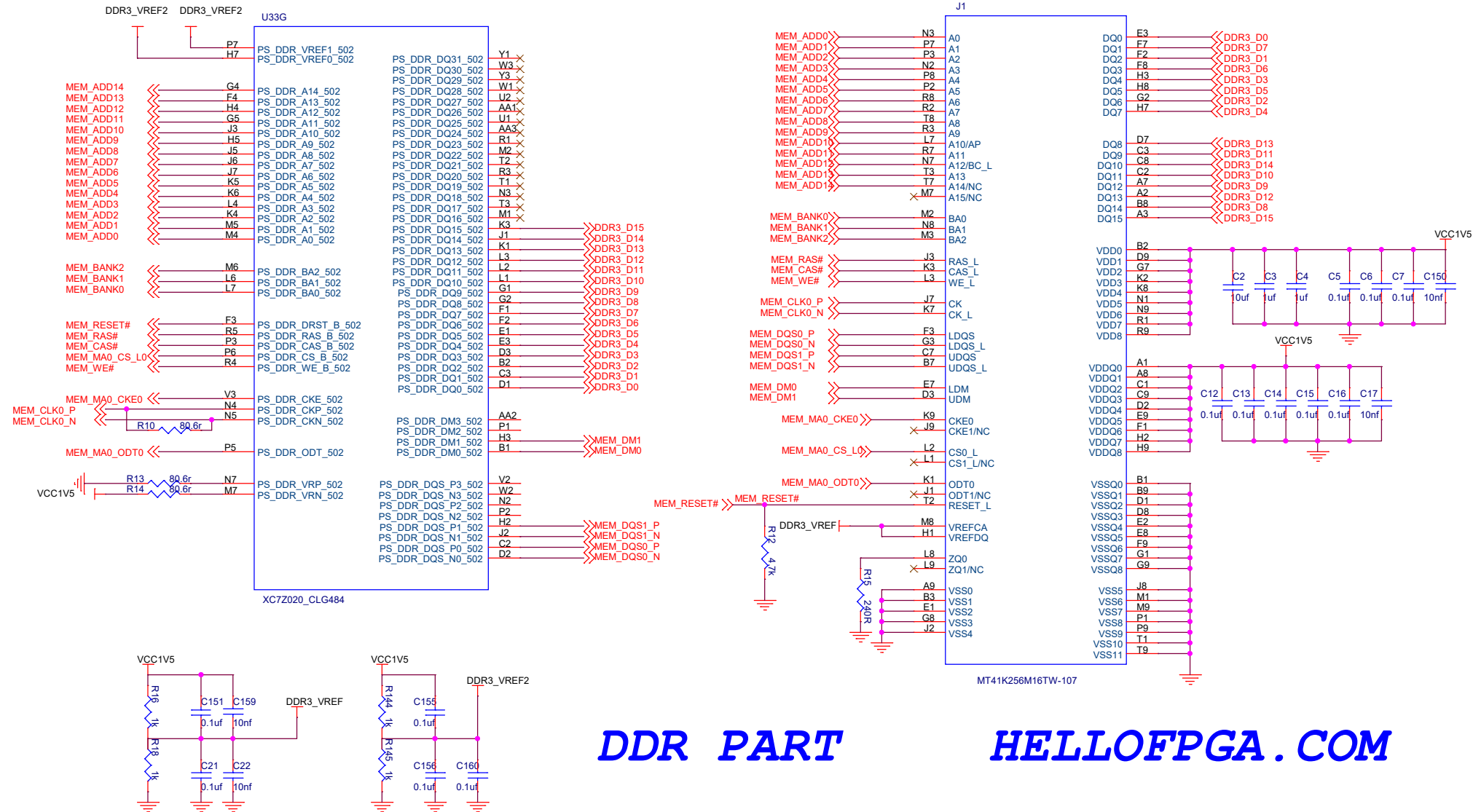


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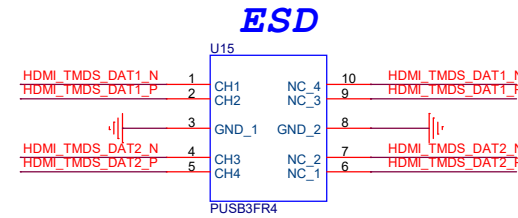
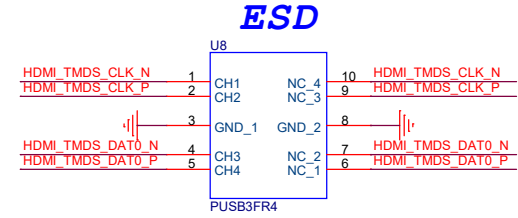
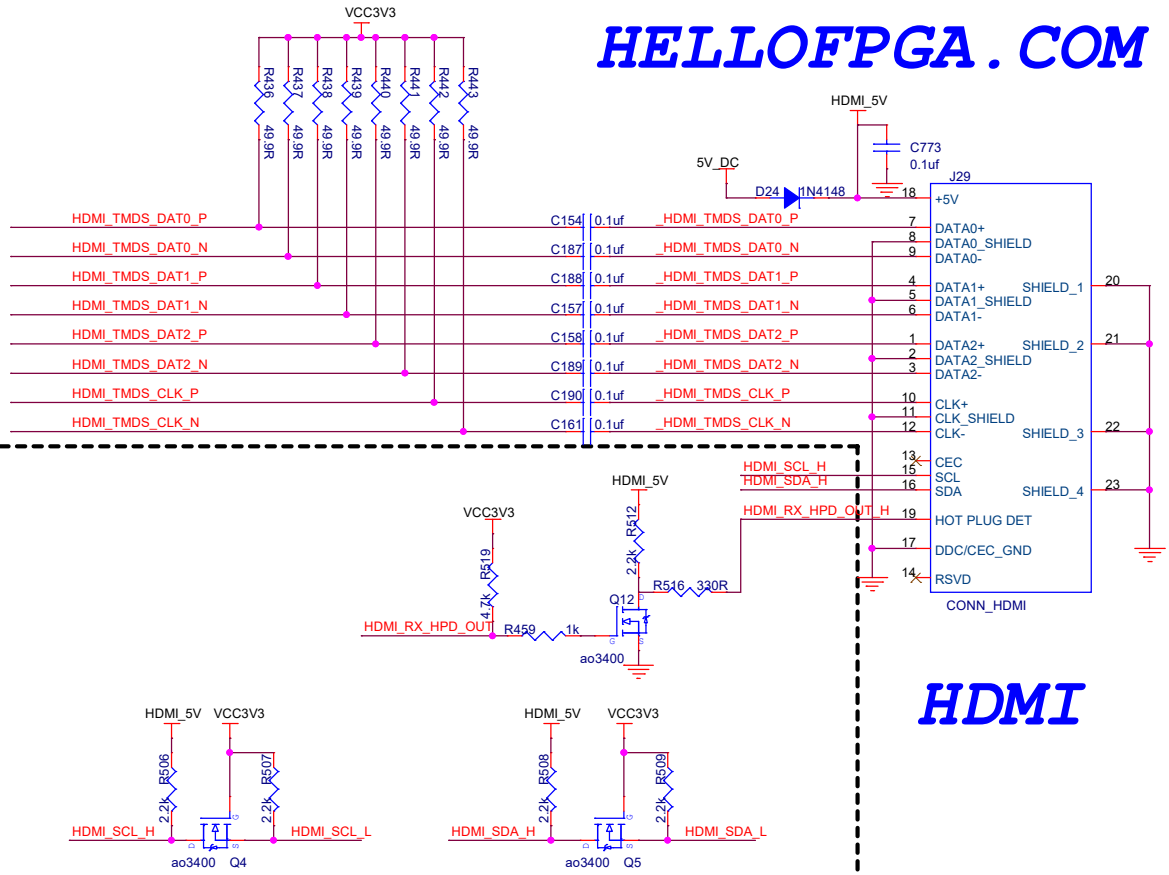
Please check the version information indicated on the silk-screen markings of the motherboard



DDR PART

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| Date: | Monday, May 01, 2023 | Sheet 1 of 1 |



HDMI

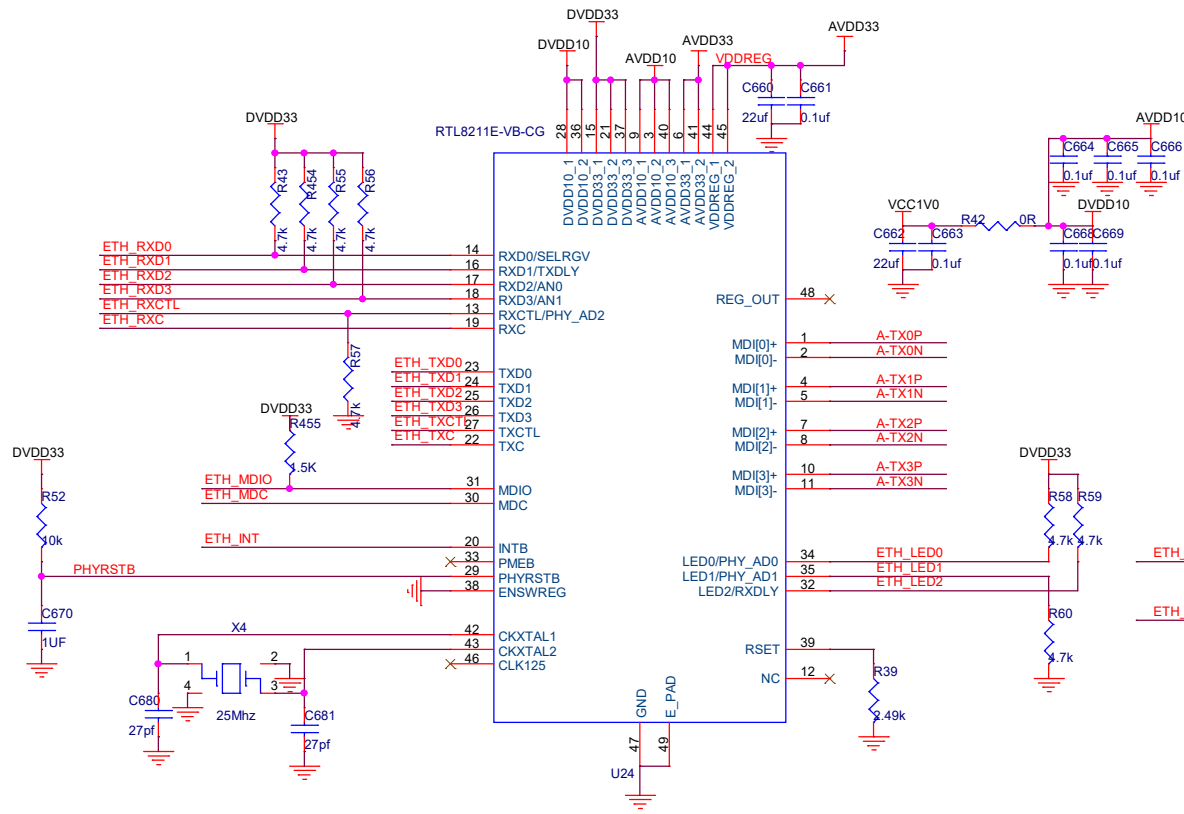
注意：v1.3版本硬件中新增HDMI SDA, HDMI SCL, RX_HPD_OUT 三个信号 (v1.1/v1.0中不存在)

Note: The circuit version 1.3 introduces three new HDMI signals SDA, SCL, and RX_HPD_OUT which are not present in circuit versions 1.1 and 1.0.

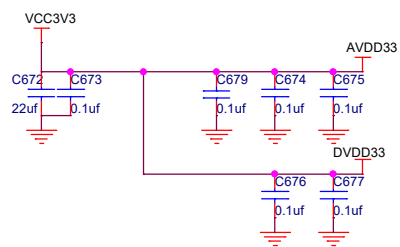
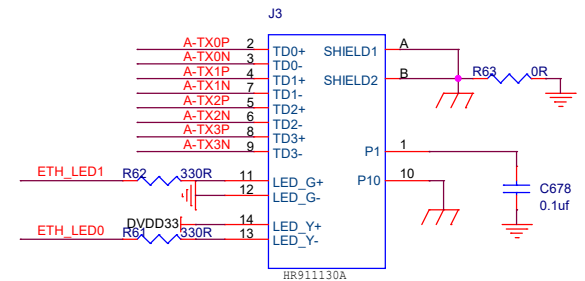
版本信息标注在主板的丝印上

Please check the version information indicated on the silk-screen markings of the motherboard

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| HELLOFPGA.COM | | |
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| Date: | Friday, August 30, 2024 | Sheet 1 of 1 |

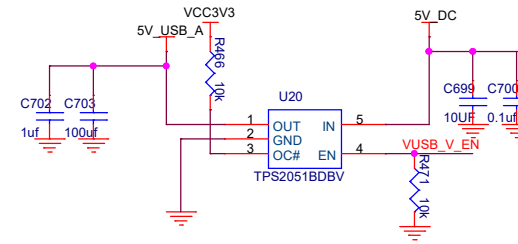
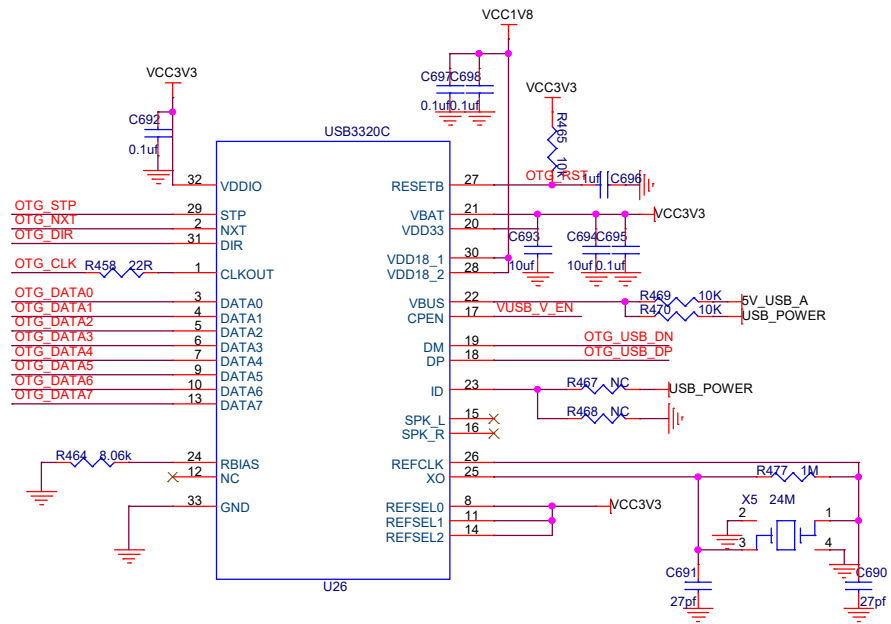


NET PART

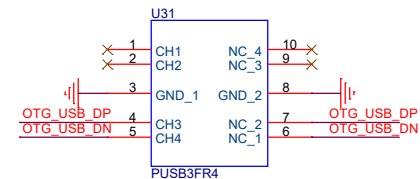
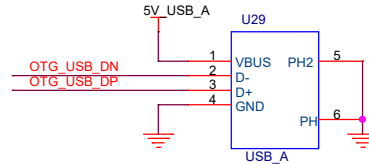
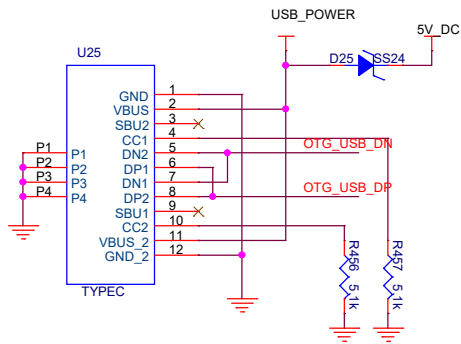


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| Size | Document Number | Rev |
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| Date: | Monday, May 01, 2023 | Sheet 1 of 1 |



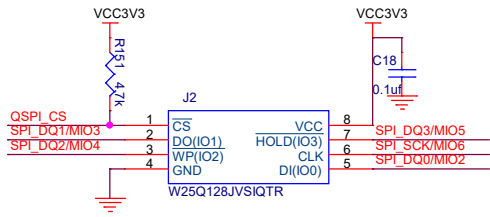
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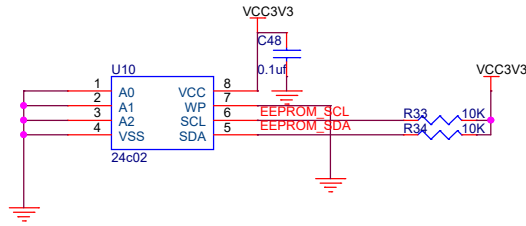
USB PART

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|---------------|----------------------|--------------|
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| HELLOFPGA.COM | | |
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| Date: | Monday, May 01, 2023 | Sheet 1 of 1 |

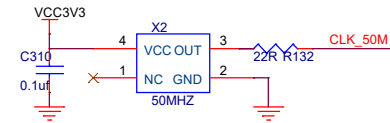
QSPI FLASH



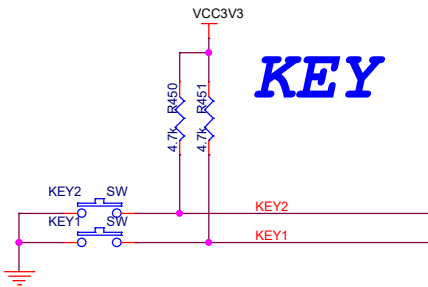
EEPROM



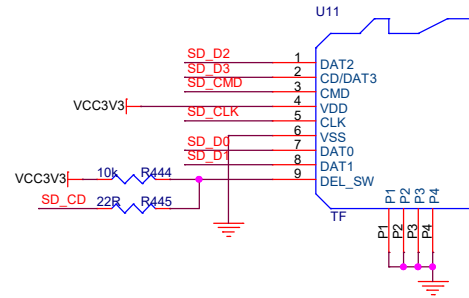
PL CLK



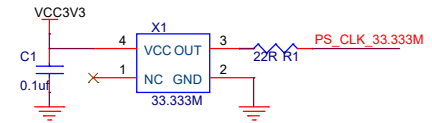
KEY



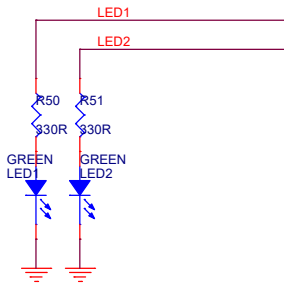
TF CARD



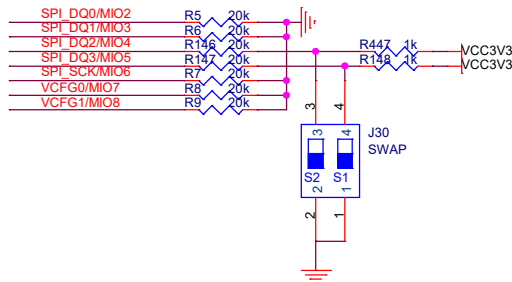
PS CLK



LED



BOOT

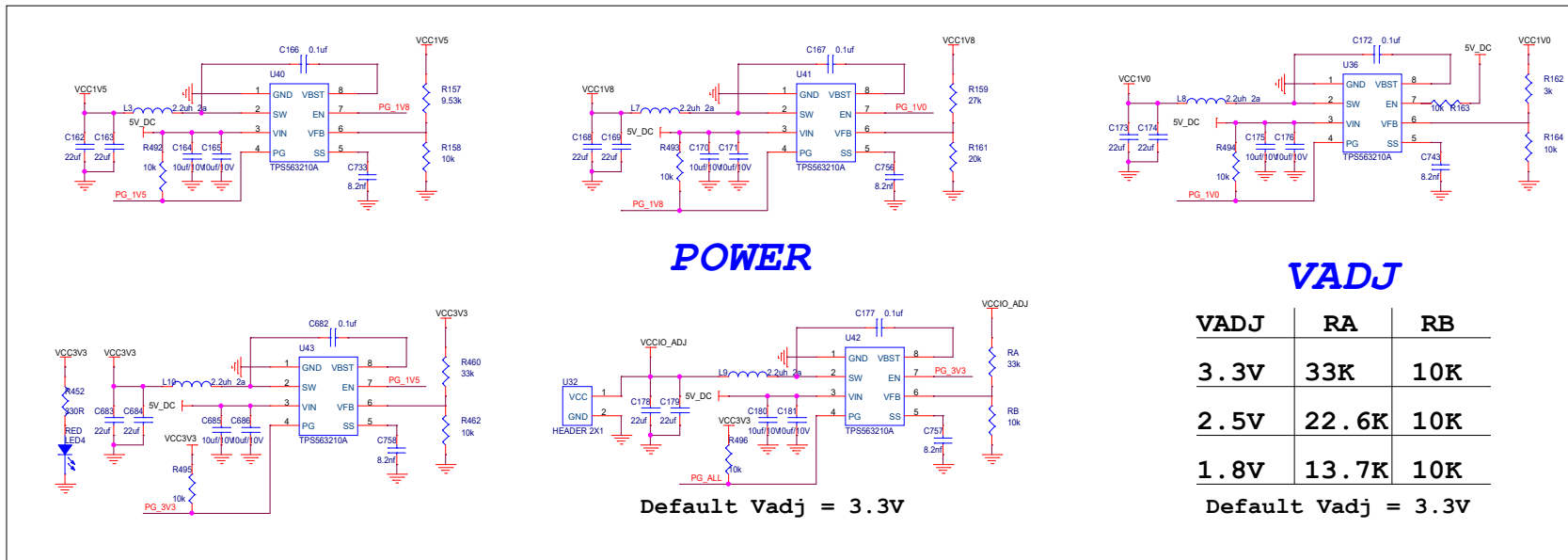


BOOT

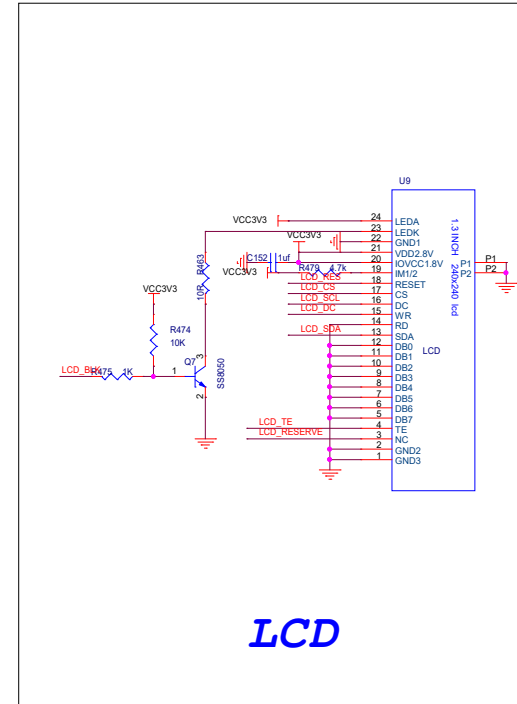
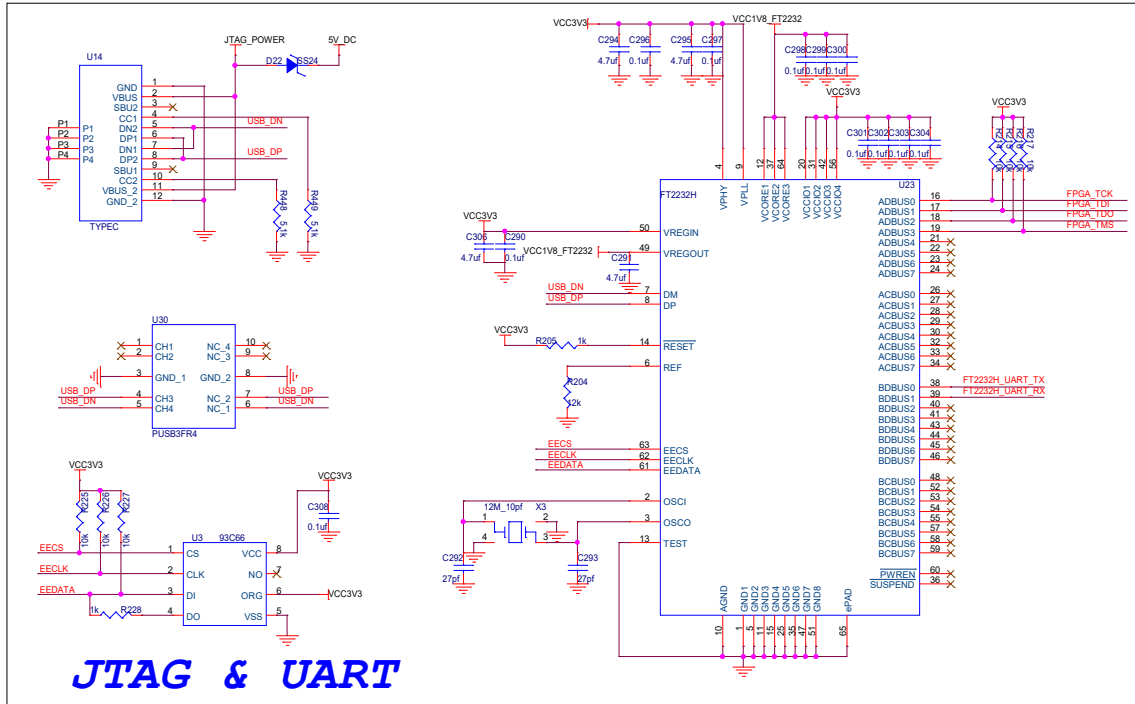
| BOOT | S1 | S2 |
|------|----|----|
| JTAG | ● | ● |
| QSPI | ○ | ● |
| SD | ○ | ○ |

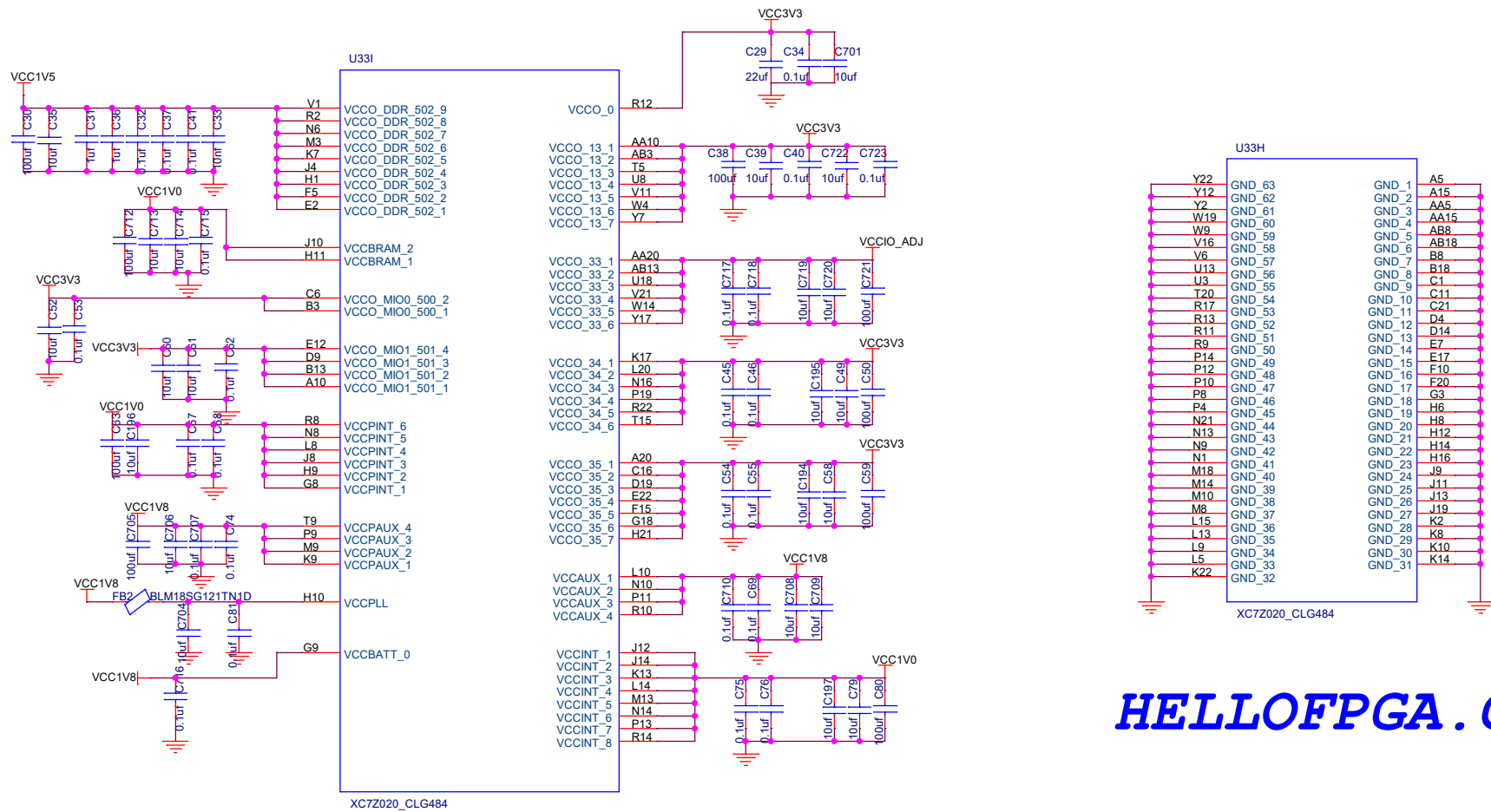
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| Title | | |
| HELLOFPGA.COM | | |
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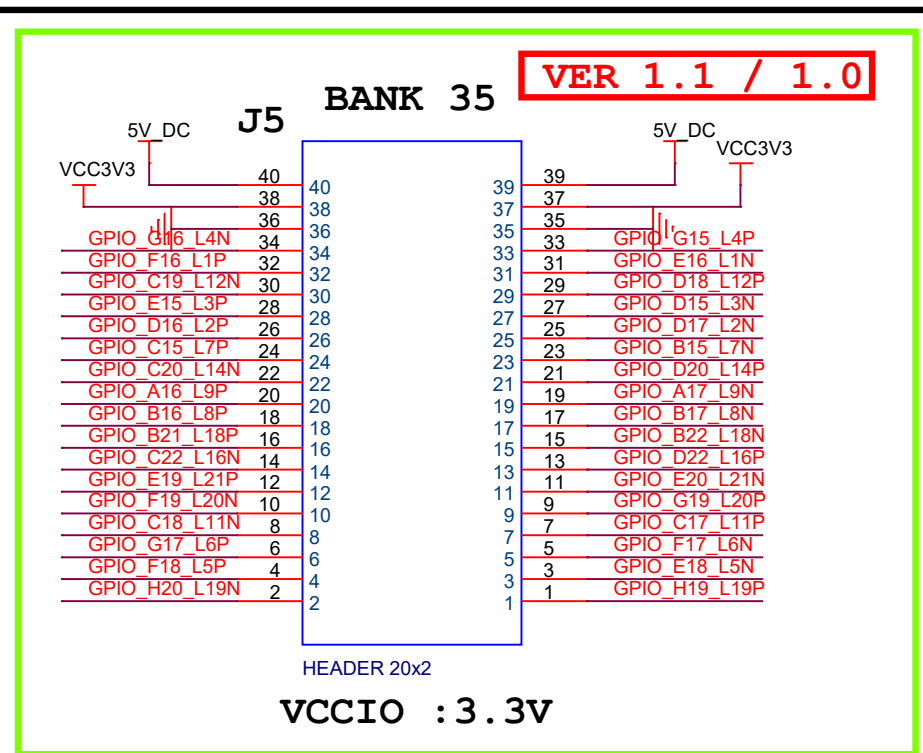
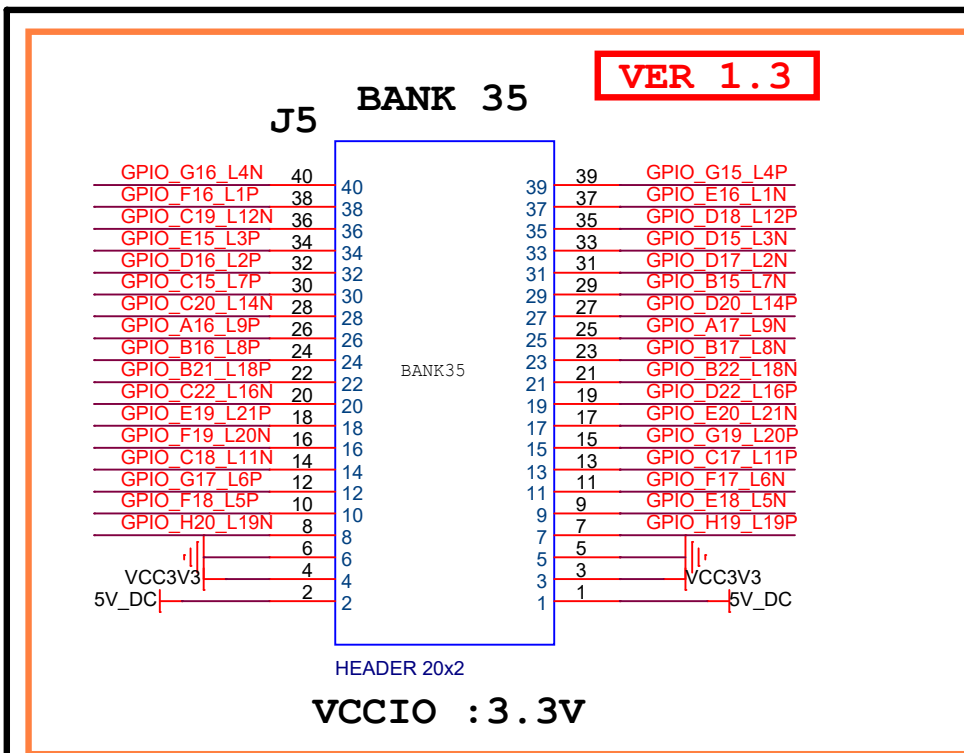
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| Date: | Monday, May 01, 2023 | Sheet 1 of 1 |

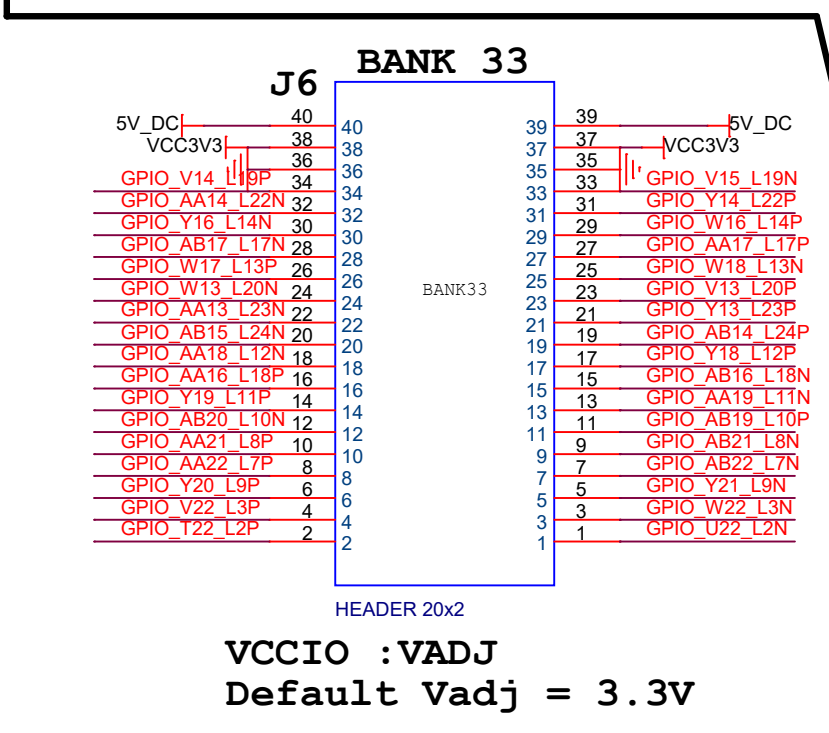


请注意：v1.3 版本的主板J5排针部分和v1.1/v1.0版本并不兼容

Please note: Version 1.3 J5 pinout is not compatible with versions 1.1/1.0.

版本信息标注在主板的丝印上

Please check the version information indicated on the silk-screen markings of the motherboard



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| Date: | Friday, August 30, 2024 | Sheet 1 of 3 |

UART

ZYNQ_TX L17

ZYNQ_RX M17

EEPROM

SCL R20

SDA R21

50M CLOCK

CLK M19

HDMI

V1.0/V1.1 V1.3

CLK N22 N19

D0 M21 M21

D1 L21 L21

D2 J21 J21

SDA / K20

SCL / K19

RX_HPD_OUT / L19

KEY & LED

KEY1 K21

KEY2 J20

LED1 P20

LED2 P21

LCD 240x240

LCD_DC R15

LCD_CS P15

LCD_SCL N15

LCD_SDA M15

LCD_RES L16

LCD_BLK T16

LCD_TE J17

(LCD BLK : default high level by
External pull-up resistance)

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GigE phy

ETH_TD0 E21

ETH_TD1 F21

ETH_TD2 F22

ETH_TD3 G20

ETH_TX_CTL G22

ETH_TXC D21

ETH_RD0 A22

ETH_RD1 A18

ETH_RD2 A19

ETH_RD3 B20

ETH_RX_CTL A21

ETH_RXC B19

ETH_MDIO H22

ETH_MDC G21

ETH_INT H18

Smart ZYNQ SP2 board Pin Constraint Definition Reference

```

create_clock -period 20 -name clk_50 [get_ports clk_50]
set_property -dict {PACKAGE_PIN M19 IOSTANDARD LVCMOS33} [get_ports clk_50]

set_property -dict {PACKAGE_PIN M17 IOSTANDARD LVCMOS33} [get_ports uart_rxd]
set_property -dict {PACKAGE_PIN L17 IOSTANDARD LVCMOS33} [get_ports uart_txd]

set_property -dict {PACKAGE_PIN P20 IOSTANDARD LVCMOS33} [get_ports LED1]
set_property -dict {PACKAGE_PIN P21 IOSTANDARD LVCMOS33} [get_ports LED2]
set_property -dict {PACKAGE_PIN K21 IOSTANDARD LVCMOS33} [get_ports KEV1]
set_property -dict {PACKAGE_PIN J20 IOSTANDARD LVCMOS33} [get_ports KEV2]

set_property -dict {PACKAGE_PIN R20 IOSTANDARD LVCMOS33} [get_ports EEPROM_SCL]
set_property -dict {PACKAGE_PIN R21 IOSTANDARD LVCMOS33} [get_ports EEPROM_SDA]

# RGMII PHY
create_clock -period 8 -name RGMII_rxc [get_ports RGMII_rxc]
set_property -dict {PACKAGE_PIN G21 IOSTANDARD LVCMOS33} [get_ports MDIO_PHY_mdc]
set_property -dict {PACKAGE_PIN H22 IOSTANDARD LVCMOS33} [get_ports MDIO_PHY_mdio_io]
set_property -dict {PACKAGE_PIN A22 IOSTANDARD LVCMOS33} [get_ports {RGMII_rd[0]}]
set_property -dict {PACKAGE_PIN A18 IOSTANDARD LVCMOS33} [get_ports {RGMII_rd[1]}]
set_property -dict {PACKAGE_PIN A19 IOSTANDARD LVCMOS33} [get_ports {RGMII_rd[2]}]
set_property -dict {PACKAGE_PIN B20 IOSTANDARD LVCMOS33} [get_ports {RGMII_rd[3]}]
set_property -dict {PACKAGE_PIN A21 IOSTANDARD LVCMOS33} [get_ports RGMII_tx_ctl1]
set_property -dict {PACKAGE_PIN B19 IOSTANDARD LVCMOS33} [get_ports RGMII_tx]
set_property -dict {PACKAGE_PIN E21 IOSTANDARD LVCMOS33} [get_ports {RGMII_td[0]}]
set_property -dict {PACKAGE_PIN F21 IOSTANDARD LVCMOS33} [get_ports {RGMII_td[1]}]
set_property -dict {PACKAGE_PIN F22 IOSTANDARD LVCMOS33} [get_ports {RGMII_td[2]}]
set_property -dict {PACKAGE_PIN G20 IOSTANDARD LVCMOS33} [get_ports {RGMII_td[3]}]
set_property -dict {PACKAGE_PIN G22 IOSTANDARD LVCMOS33} [get_ports RGMII_tx_ctl1]
set_property -dict {PACKAGE_PIN D21 IOSTANDARD LVCMOS33} [get_ports RGMII_tx]
set_property SLEW FAST [get_ports {RGMII_td[0]}]
set_property SLEW FAST [get_ports {RGMII_td[1]}]
set_property SLEW FAST [get_ports {RGMII_td[2]}]
set_property SLEW FAST [get_ports {RGMII_td[3]}]
set_property SLEW FAST [get_ports RGMII_tx_ctl1]
set_property SLEW FAST [get_ports RGMII_tx]

```

```

# VBR V1.0 / V1.1
# HDMI (DVI) outputs
set_property PACKAGE_PIN J21 [get_ports {hdmi_d_p[2]}]
set_property PACKAGE_PIN L21 [get_ports {hdmi_d_p[1]}]
set_property PACKAGE_PIN M21 [get_ports {hdmi_d_p[0]}]
set_property PACKAGE_PIN N22 [get_ports hdmi_clk_p]

# VBR V1.3
# HDMI (DVI) outputs
set_property PACKAGE_PIN J21 [get_ports {hdmi_d_p[2]}]
set_property PACKAGE_PIN L21 [get_ports {hdmi_d_p[1]}]
set_property PACKAGE_PIN M21 [get_ports {hdmi_d_p[0]}]

set_property PACKAGE_PIN N19 [get_ports hdmi_clk_p]
set_property -dict {PACKAGE_PIN K20 IOSTANDARD LVCMOS33} [get_ports HDMI_SDA]
set_property -dict {PACKAGE_PIN K19 IOSTANDARD LVCMOS33} [get_ports HDMI_SCL]
set_property -dict {PACKAGE_PIN L19 IOSTANDARD LVCMOS33} [get_ports HDMI_RX_HPD]

```

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```

## J5 on board (BANK35 V3V3)
# Set voltage level for banks35 (match with jumper setting on board)
set_property IOSTANDARD LVCMOS33 [get_ports {J5[*]}]
set_property PACKAGE_PIN H19 [get_ports {J5[0]}]; #IO B35_LP19
set_property PACKAGE_PIN H20 [get_ports {J5[1]}]; #IO B35_LN19
set_property PACKAGE_PIN E18 [get_ports {J5[2]}]; #IO B35_LN5
set_property PACKAGE_PIN F18 [get_ports {J5[3]}]; #IO B35_LP5
set_property PACKAGE_PIN F17 [get_ports {J5[4]}]; #IO B35_LN6
set_property PACKAGE_PIN G17 [get_ports {J5[5]}]; #IO B35_LP6
set_property PACKAGE_PIN C17 [get_ports {J5[6]}]; #IO B35_LP11
set_property PACKAGE_PIN C18 [get_ports {J5[7]}]; #IO B35_LN11
set_property PACKAGE_PIN G19 [get_ports {J5[8]}]; #IO B35_LP20
set_property PACKAGE_PIN F19 [get_ports {J5[9]}]; #JIO B35_LN20
set_property PACKAGE_PIN E20 [get_ports {J5[10]}]; #IO B35_LN21
set_property PACKAGE_PIN E19 [get_ports {J5[11]}]; #IO B35_LP21
set_property PACKAGE_PIN D22 [get_ports {J5[12]}]; #IO B35_LP16
set_property PACKAGE_PIN C22 [get_ports {J5[13]}]; #IO B35_LN16
set_property PACKAGE_PIN B22 [get_ports {J5[14]}]; #IO B35_LN18
set_property PACKAGE_PIN B21 [get_ports {J5[15]}]; #IO B35_LP18
set_property PACKAGE_PIN B17 [get_ports {J5[16]}]; #IO B35_LN8
set_property PACKAGE_PIN B16 [get_ports {J5[17]}]; #IO B35_LP8
set_property PACKAGE_PIN A17 [get_ports {J5[18]}]; #IO B35_LN9
set_property PACKAGE_PIN A16 [get_ports {J5[19]}]; #IO B35_LP9
set_property PACKAGE_PIN D20 [get_ports {J5[20]}]; #IO B35_LP14
set_property PACKAGE_PIN C20 [get_ports {J5[21]}]; #IO B35_LN14
set_property PACKAGE_PIN B15 [get_ports {J5[22]}]; #IO B35_LN7
set_property PACKAGE_PIN C15 [get_ports {J5[23]}]; #IO B35_LP7
set_property PACKAGE_PIN D17 [get_ports {J5[24]}]; #IO B35_LN2
set_property PACKAGE_PIN D16 [get_ports {J5[25]}]; #IO B35_LP2
set_property PACKAGE_PIN D15 [get_ports {J5[26]}]; #IO B35_LN3
set_property PACKAGE_PIN E15 [get_ports {J5[27]}]; #IO B35_LP3
set_property PACKAGE_PIN D18 [get_ports {J5[28]}]; #IO B35_LP12
set_property PACKAGE_PIN C15 [get_ports {J5[29]}]; #IO B35_LN12
set_property PACKAGE_PIN E16 [get_ports {J5[30]}]; #IO B35_LN1
set_property PACKAGE_PIN F16 [get_ports {J5[31]}]; #IO B35_LP1
set_property PACKAGE_PIN G15 [get_ports {J5[32]}]; #IO B35_LP4
set_property PACKAGE_PIN G16 [get_ports {J5[33]}]; #IO B35_LN4

```

```

## J6 on board (BANK33 VADJ)
# Set voltage level for banks 33 (match with jumper setting on board)
set_property IOSTANDARD LVCMOS33 [get_ports {J6[*]}]
set_property PACKAGE_PIN U22 [get_ports {J6[0]}]; #J6/1 = IO B33_LM2
set_property PACKAGE_PIN V22 [get_ports {J6[1]}]; #J6/2 = IO B33_LP2
set_property PACKAGE_PIN W22 [get_ports {J6[2]}]; #J6/3 = IO B33_LM3
set_property PACKAGE_PIN V22 [get_ports {J6[3]}]; #J6/4 = IO B33_LP3
set_property PACKAGE_PIN V21 [get_ports {J6[4]}]; #J6/5 = IO B33_LM9
set_property PACKAGE_PIN V20 [get_ports {J6[5]}]; #J6/6 = IO B33_LP9
set_property PACKAGE_PIN AB22 [get_ports {J6[6]}]; #J6/7 = IO B33_LM7
set_property PACKAGE_PIN AA22 [get_ports {J6[7]}]; #J6/8 = IO B33_LP7
set_property PACKAGE_PIN AB21 [get_ports {J6[8]}]; #J6/9 = IO B33_LM8
set_property PACKAGE_PIN AA21 [get_ports {J6[9]}]; #J6/10 = IO B33_LP8
set_property PACKAGE_PIN AB19 [get_ports {J6[10]}]; #J6/11 = IO B33_LP10
set_property PACKAGE_PIN AB20 [get_ports {J6[11]}]; #J6/12 = IO B33_LM10
set_property PACKAGE_PIN AA19 [get_ports {J6[12]}]; #J6/13 = IO B33_LM11
set_property PACKAGE_PIN V19 [get_ports {J6[13]}]; #J6/14 = IO B33_LP11
set_property PACKAGE_PIN AB16 [get_ports {J6[14]}]; #J6/15 = IO B33_LM18
set_property PACKAGE_PIN AA16 [get_ports {J6[15]}]; #J6/16 = IO B33_LP18
set_property PACKAGE_PIN V18 [get_ports {J6[16]}]; #J6/17 = IO B33_LP12
set_property PACKAGE_PIN AA18 [get_ports {J6[17]}]; #J6/18 = IO B33_LM12
set_property PACKAGE_PIN AB14 [get_ports {J6[18]}]; #J6/19 = IO B33_LP24
set_property PACKAGE_PIN AB15 [get_ports {J6[19]}]; #J6/20 = IO B33_LM24
set_property PACKAGE_PIN V13 [get_ports {J6[20]}]; #J6/21 = IO B33_LP23
set_property PACKAGE_PIN AA13 [get_ports {J6[21]}]; #J6/22 = IO B33_LM23
set_property PACKAGE_PIN V13 [get_ports {J6[22]}]; #J6/23 = IO B33_LP20
set_property PACKAGE_PIN W13 [get_ports {J6[23]}]; #J6/24 = IO B33_LM20
set_property PACKAGE_PIN W18 [get_ports {J6[24]}]; #J6/25 = IO B33_LM13
set_property PACKAGE_PIN W17 [get_ports {J6[25]}]; #J6/26 = IO B33_LP13
set_property PACKAGE_PIN AA17 [get_ports {J6[26]}]; #J6/27 = IO B33_LP17
set_property PACKAGE_PIN AB17 [get_ports {J6[27]}]; #J6/28 = IO B33_LM17
set_property PACKAGE_PIN W16 [get_ports {J6[28]}]; #J6/29 = IO B33_LP14
set_property PACKAGE_PIN V16 [get_ports {J6[29]}]; #J6/30 = IO B33_LM14
set_property PACKAGE_PIN V14 [get_ports {J6[30]}]; #J6/31 = IO B33_LP22
set_property PACKAGE_PIN AA14 [get_ports {J6[31]}]; #J6/32 = IO B33_LM22
set_property PACKAGE_PIN V15 [get_ports {J6[32]}]; #J6/33 = IO B33_LM19
set_property PACKAGE_PIN V14 [get_ports {J6[33]}]; #J6/34 = IO B33_LP19

```

| | | |
|-------|-------------------------|--------------|
| Title | | <Title> |
| Size | Document Number | Rev |
| B | <Doc> | <RevCode> |
| Date: | Friday, August 30, 2024 | Sheet 1 of 1 |