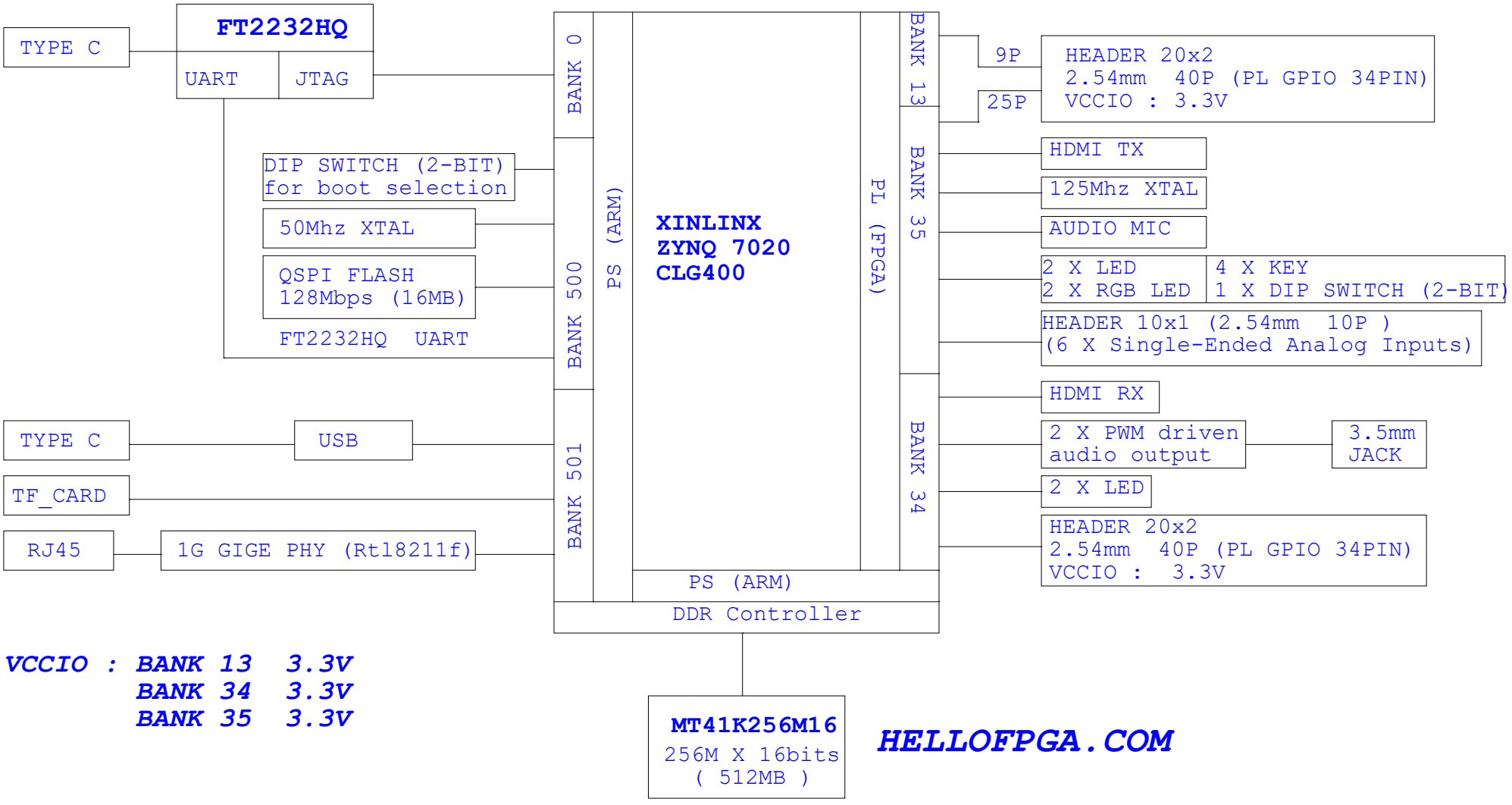
Lemon ZYNQ V1.0
Block Diagram



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BANK 35 3.3V

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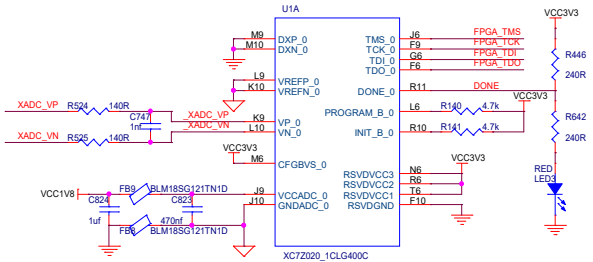

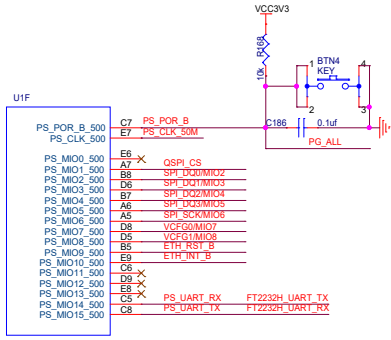

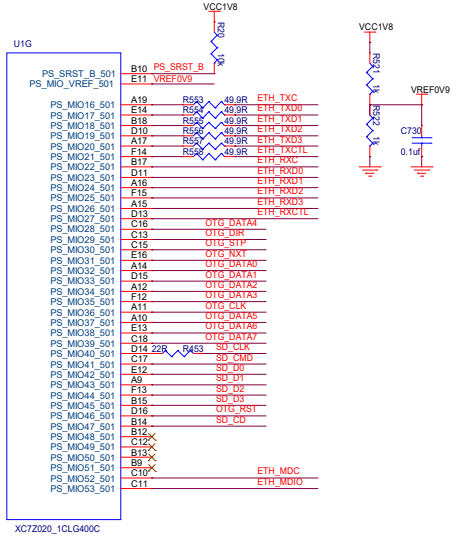

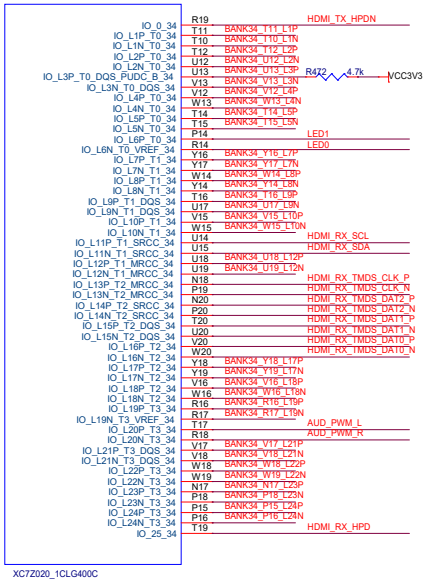

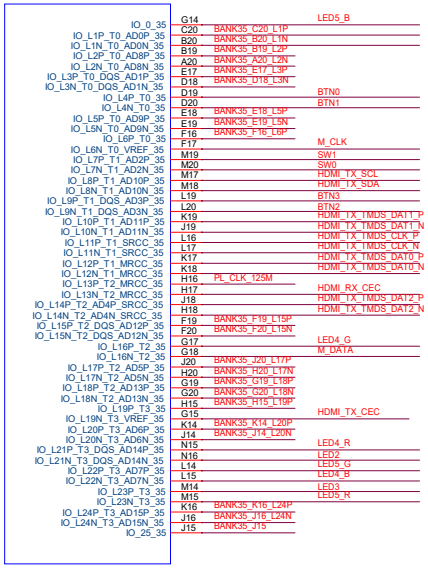

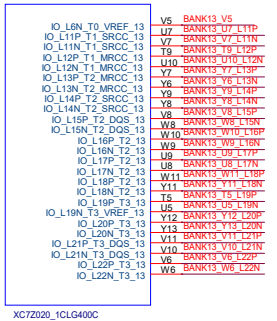

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MEM_ADD2
MEM_ADD1
MEM_ADD0
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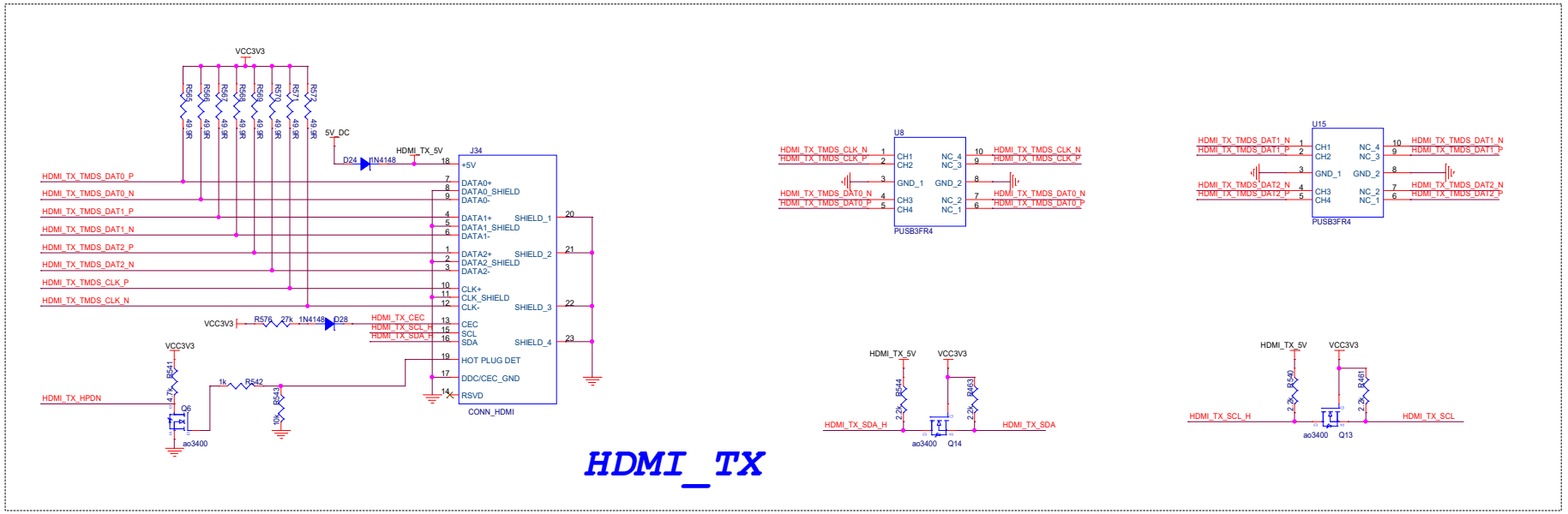

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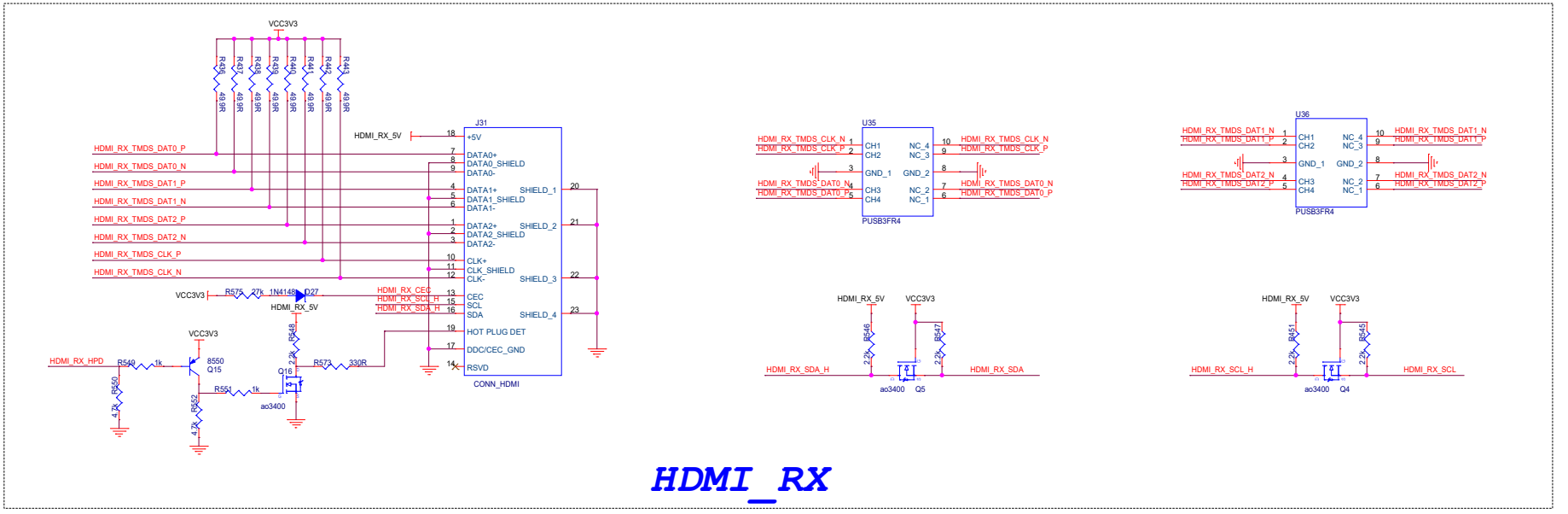

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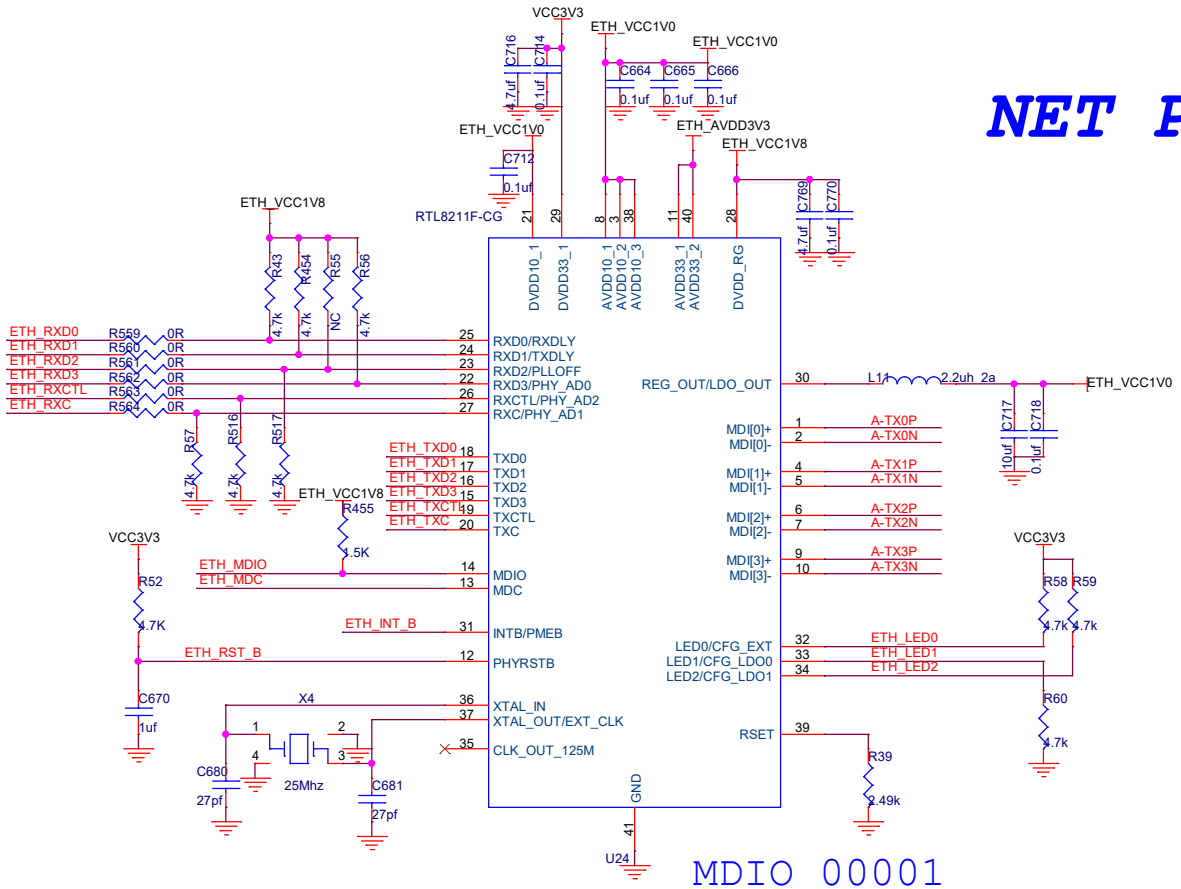

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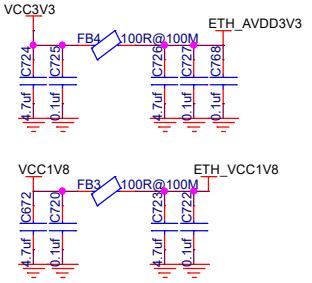

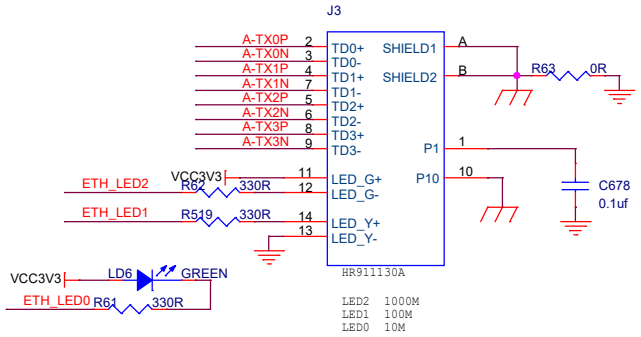

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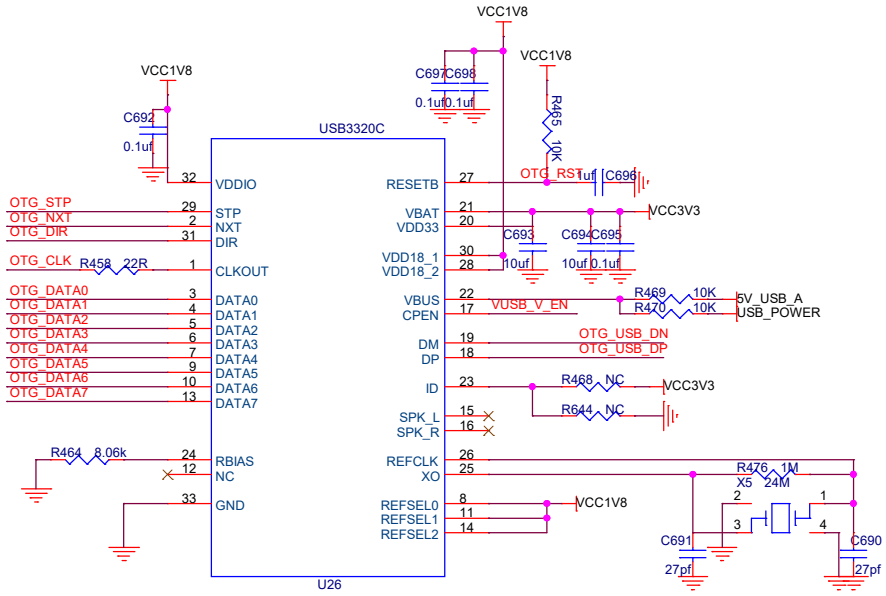

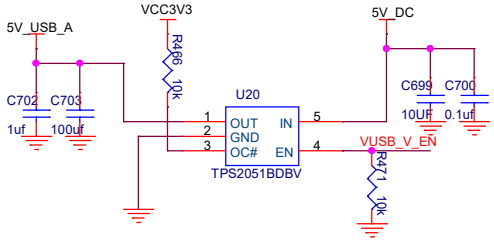

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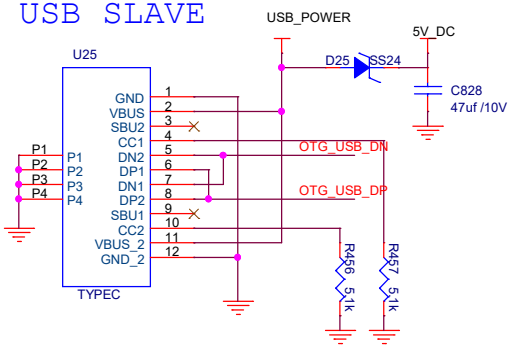

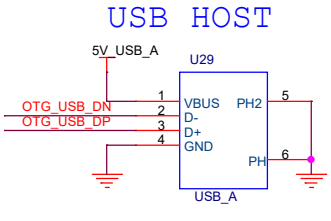

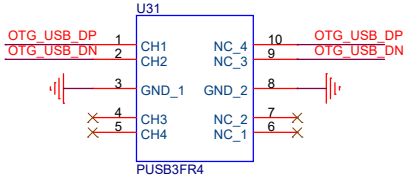

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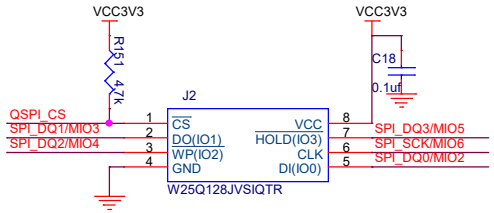

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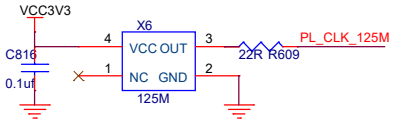

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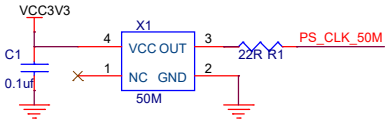

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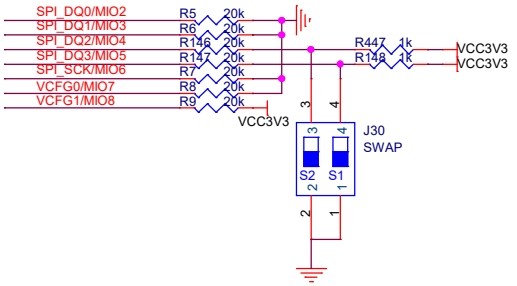

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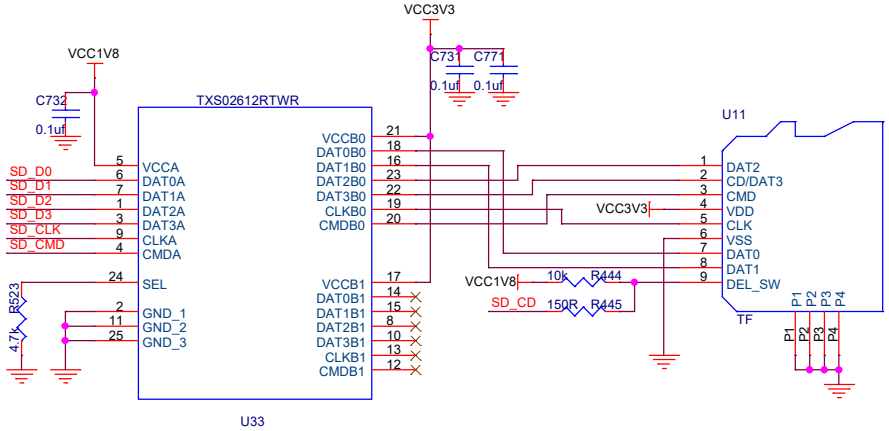

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BOOT

BOOT	S1	S2
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QSPI	○	●
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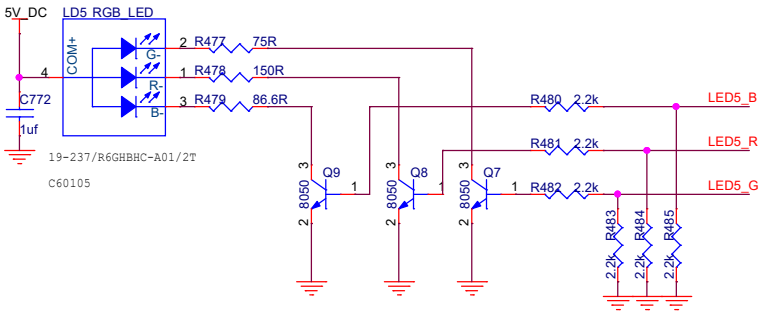

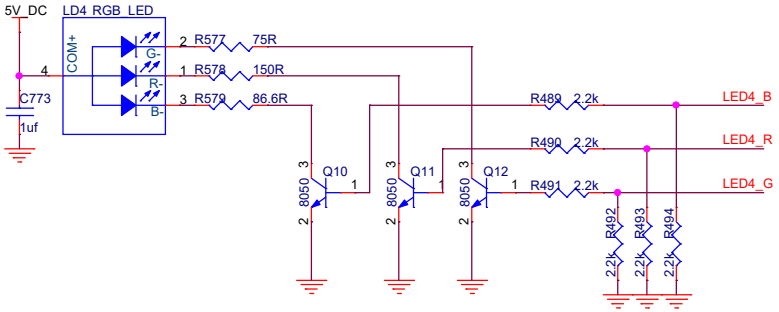

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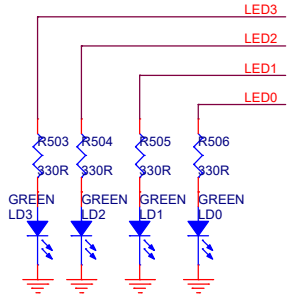

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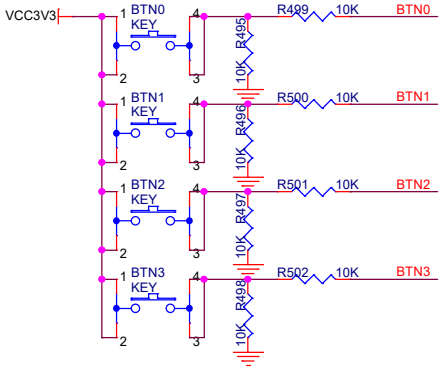

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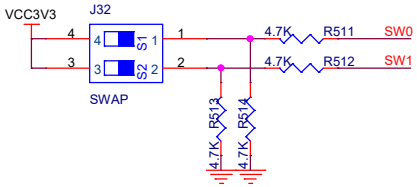

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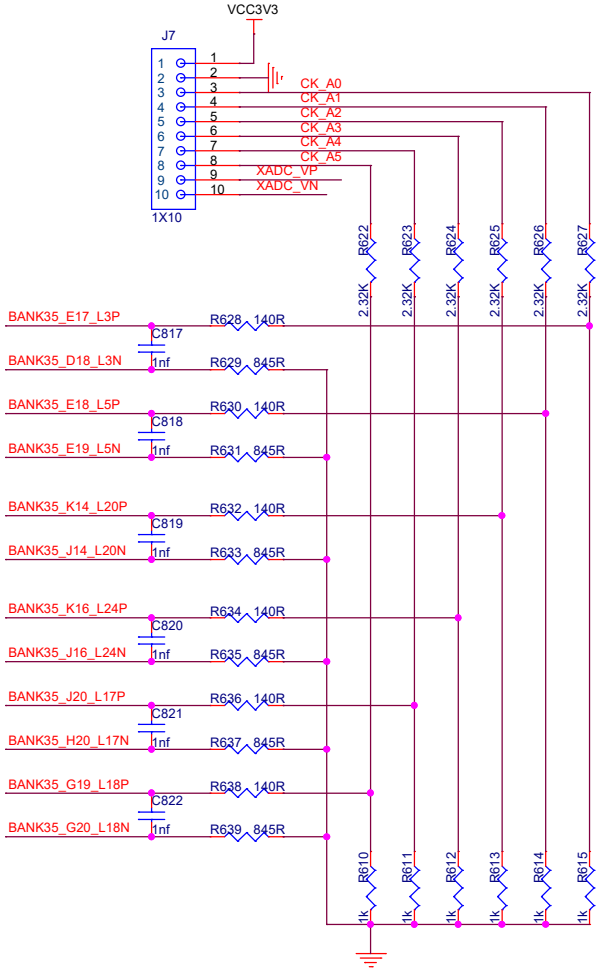

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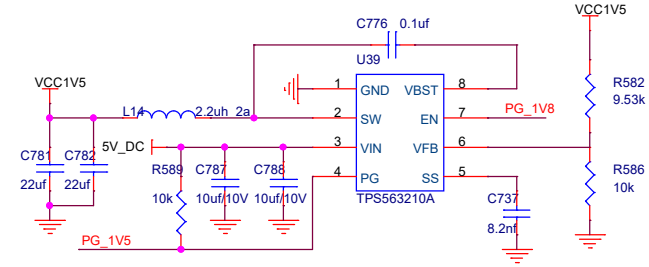

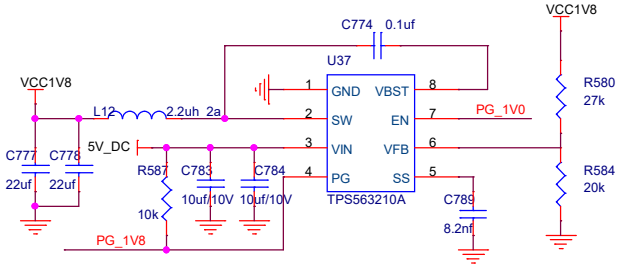

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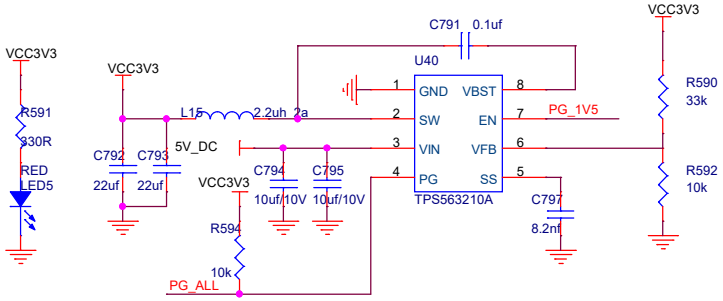

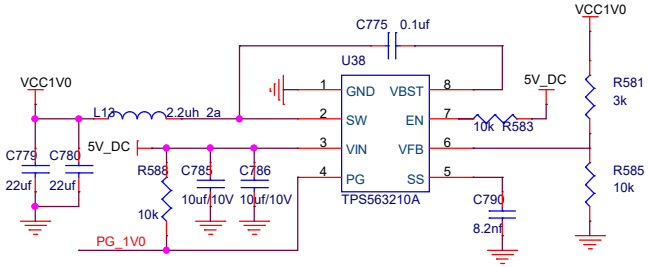

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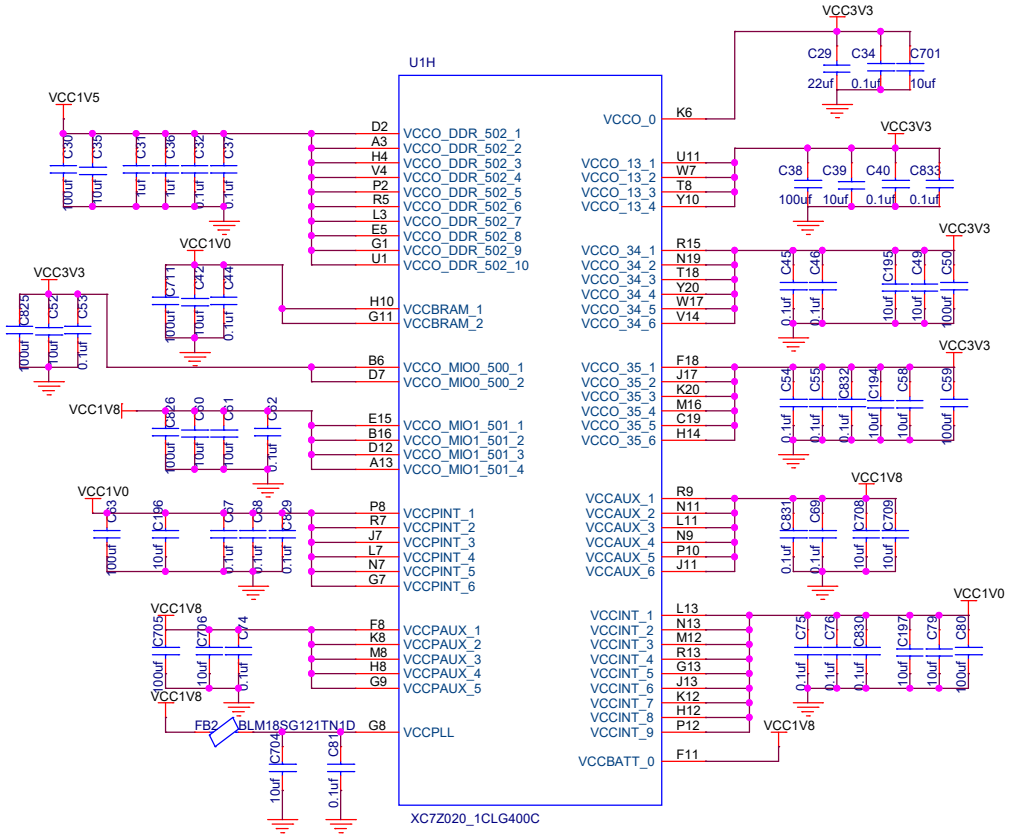

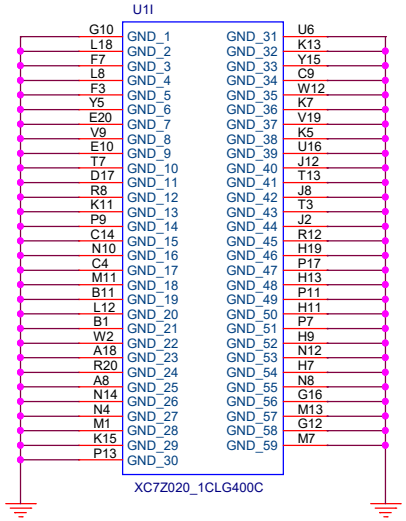

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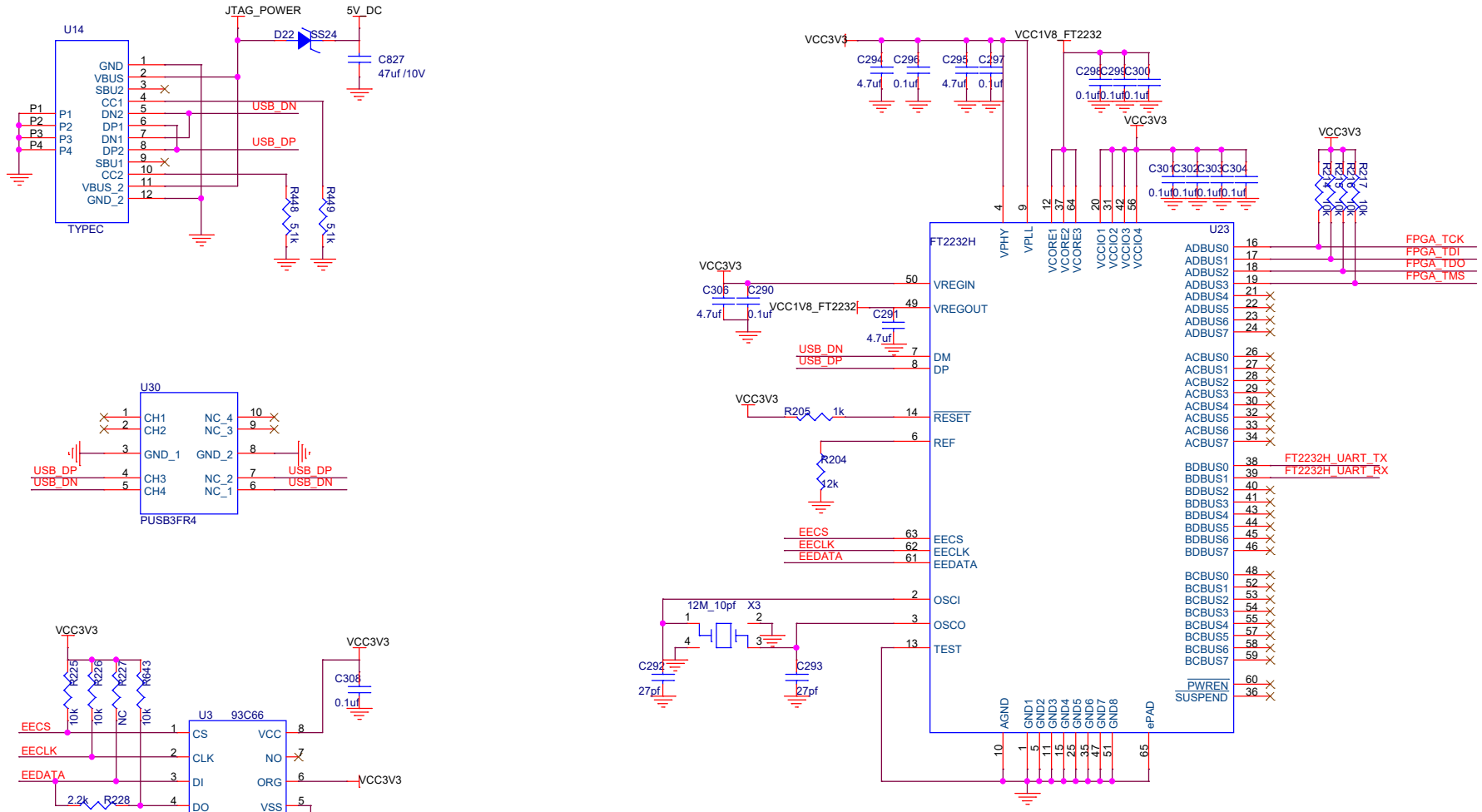

JTAG & UART

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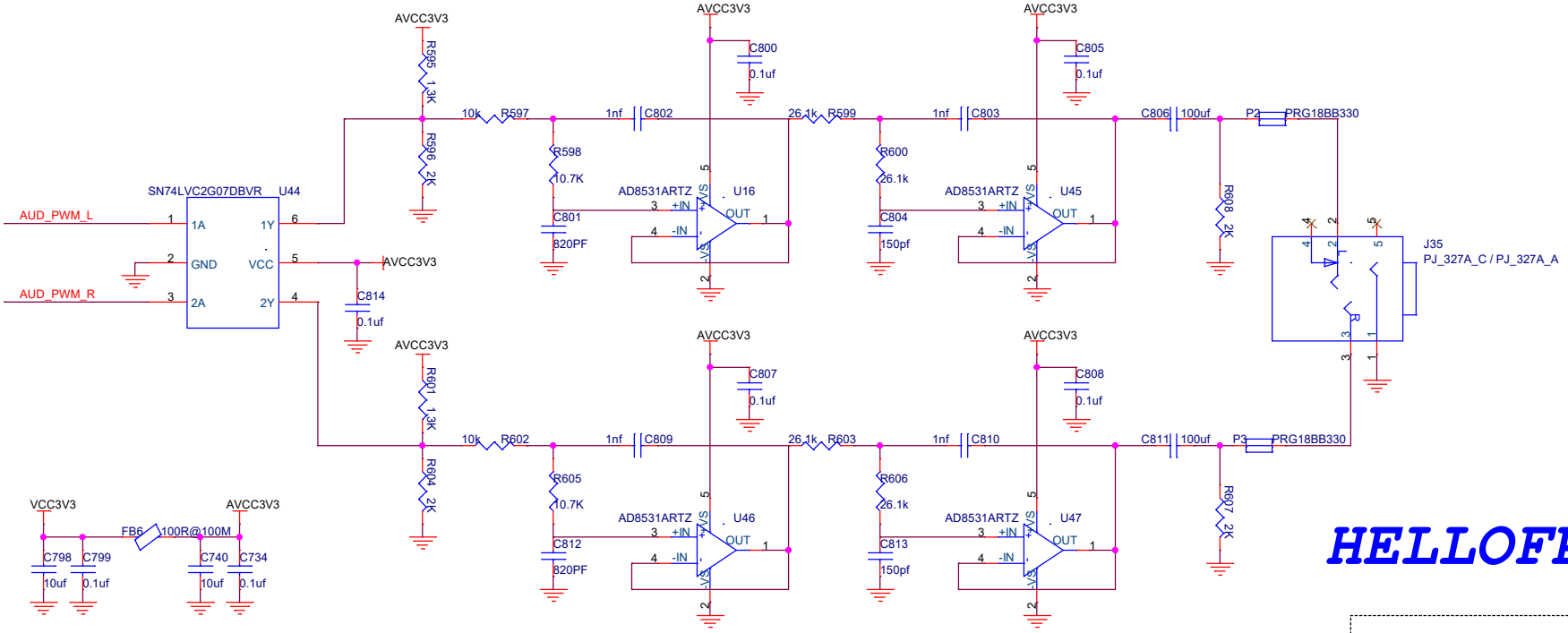
Sallen-Key Butterworth Low Pass 4th Order Filter



fc = 12.5KHz
G = 1

fc = 16.3KHz
G = 1

AUDIO_OUT

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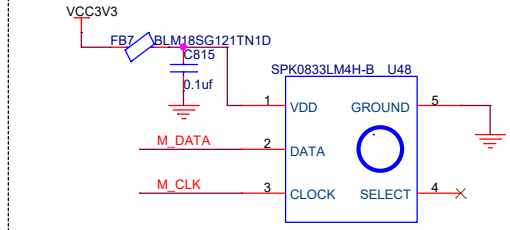

MIC

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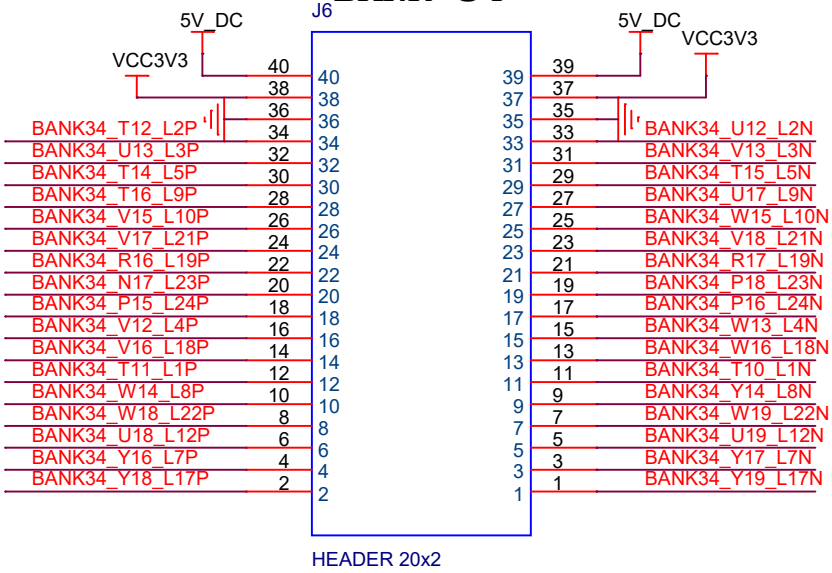
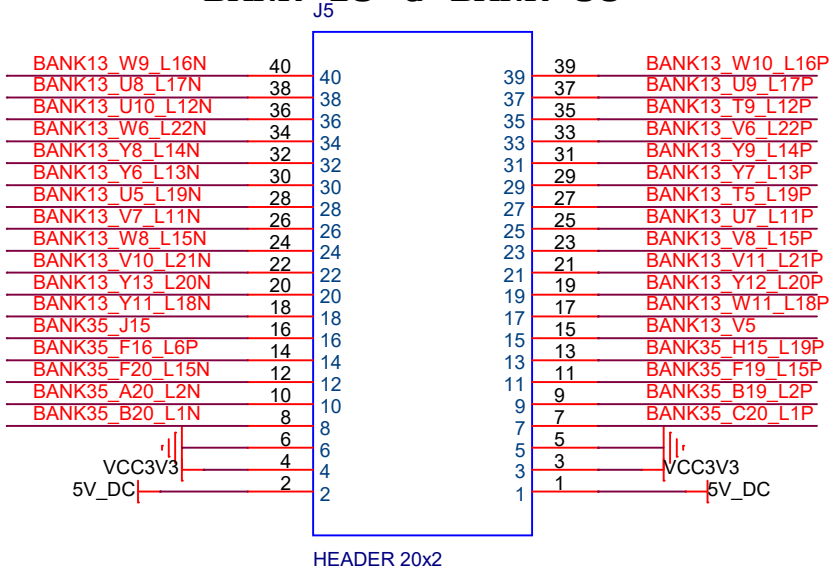
BANK 34

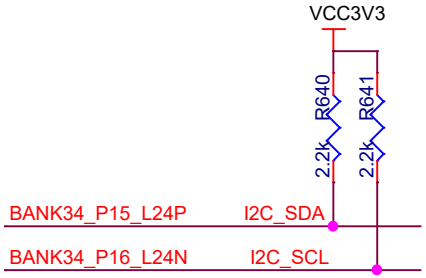


VCCIO :3.3V

BANK 13 & BANK 35



VCCIO :3.3V



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UART

ZYNQ_TX	MIO15
ZYNQ_RX	MIO14

125M CLOCK

CLK	H16

GigE phy

ETH TD0	MIO17
ETH TD1	MIO18
ETH TD2	MIO19
ETH TD3	MIO20
ETH TX_CTL	MIO21
ETH TXC	MIO16
ETH RD0	MIO23
ETH RD1	MIO24
ETH RD2	MIO25
ETH RD3	MIO26
ETH RX_CTL	MIO27
ETH RXC	MIO22
ETH MDIO	MIO53
ETH MDC	MIO52
ETH INT	MIO10
ETH RST	MIO9

KEY

BTN0	D19
BTN1	D20
BTN2	L20
BTN3	L19

LED

LD0	R14
LD1	P14
LD2	N16
LD3	M14

RGB LED

	LD5	LD4
R	M15	N15
G	L14	G17
B	G14	L15

MIC

M_DATA	G18
M_CLK	F17

AUDIO OUT

AUD_PWM_L	T17
AUD_PWM_R	R18

DIP SWITCH

SW1	M19
SW0	M20

HDMI

	RX	TX
CLK	N18	L16
D0	V20	K17
D1	T20	K19
D2	N20	J18
SDA	U15	M18
SCL	U14	M17
HPD	T19	R19

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